

P25Z PG611 A00

12GB GDDR5X, 384b, 256Mx32


TALL DVI-D + DP + DP + HDMI/DP + DP

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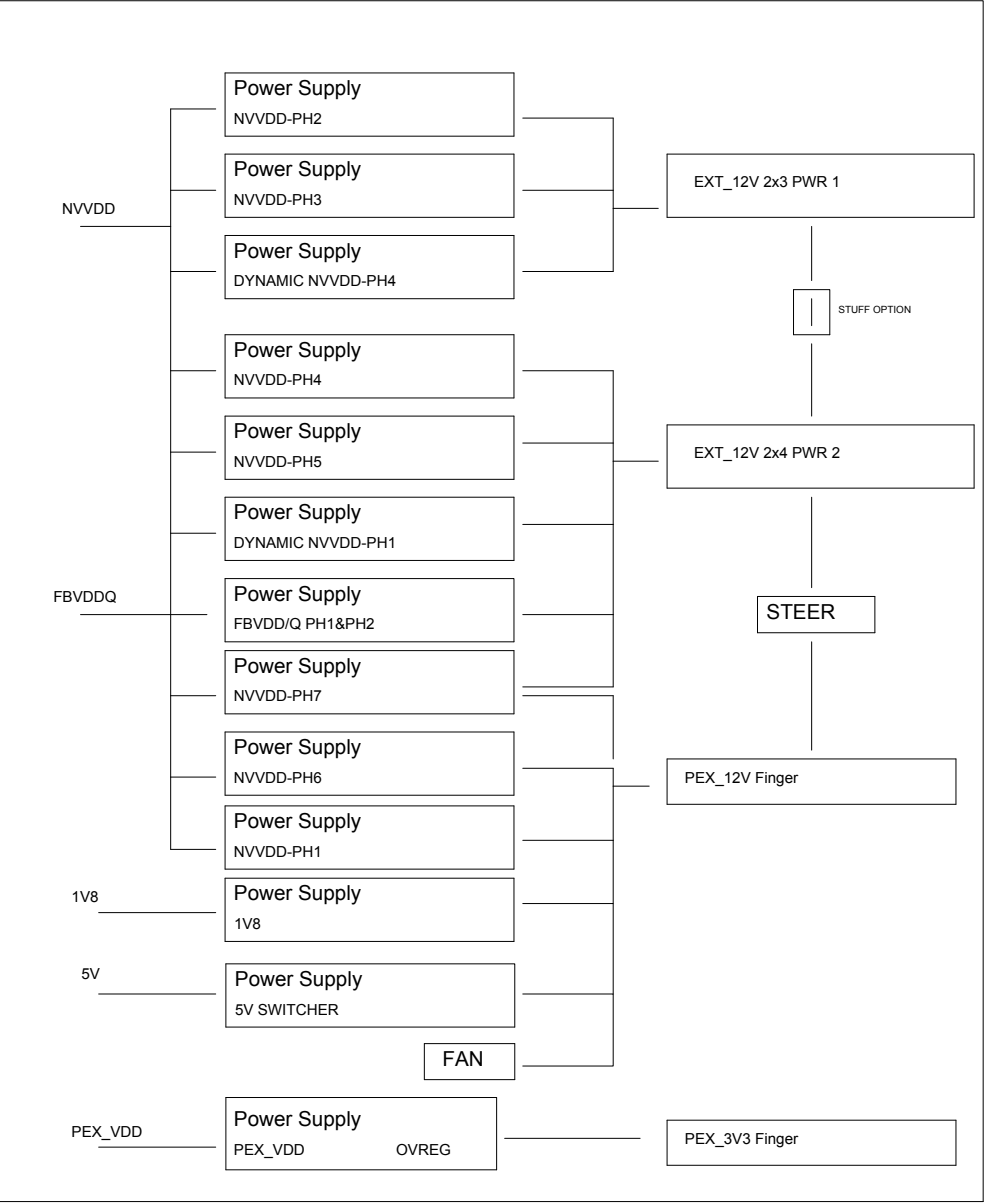
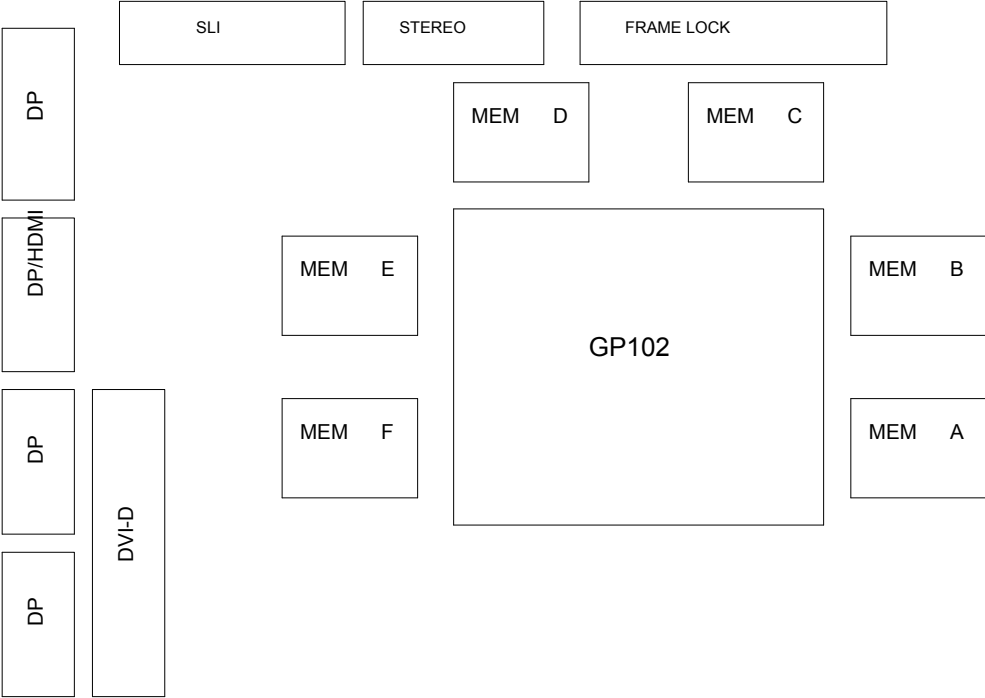
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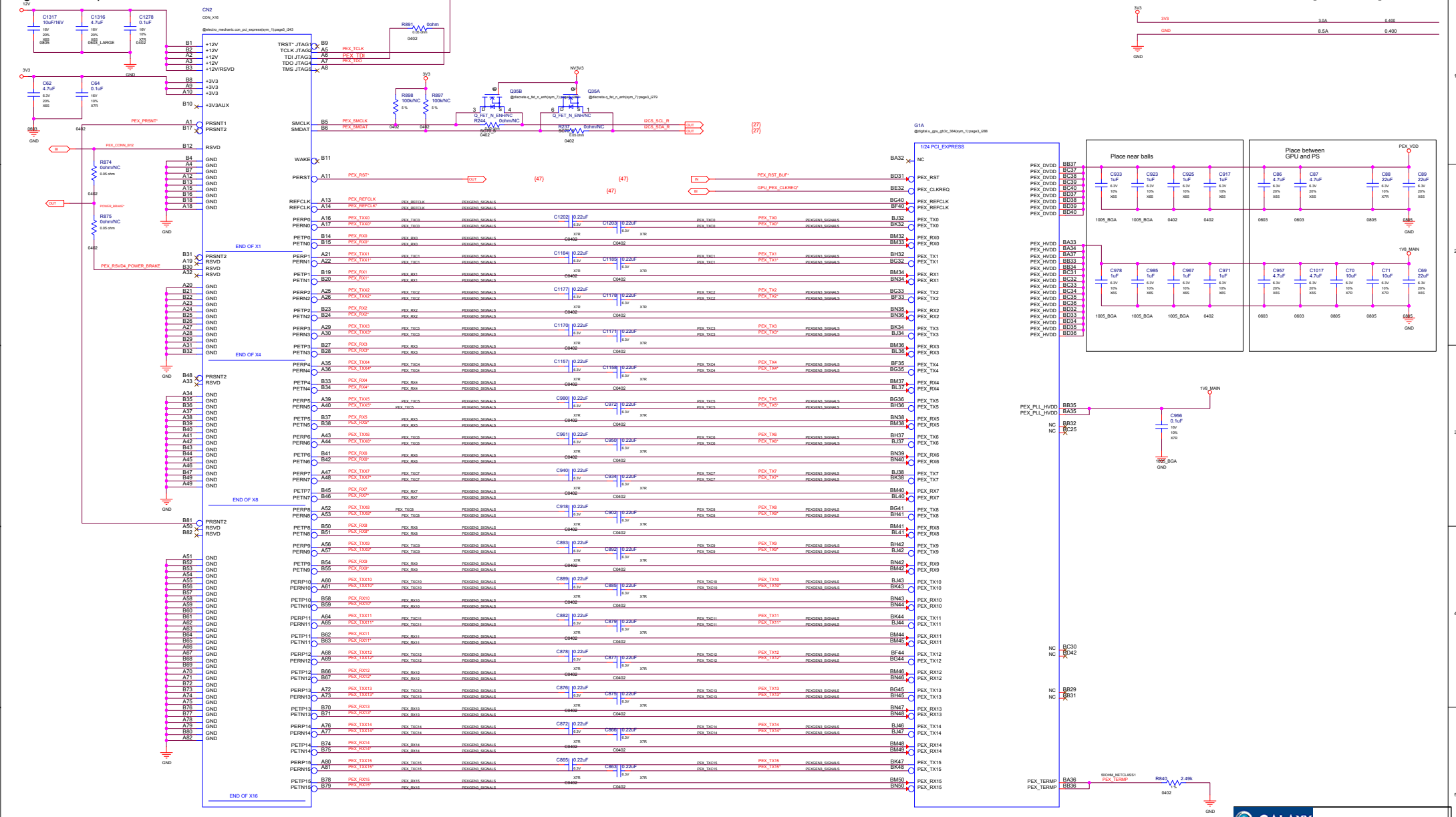
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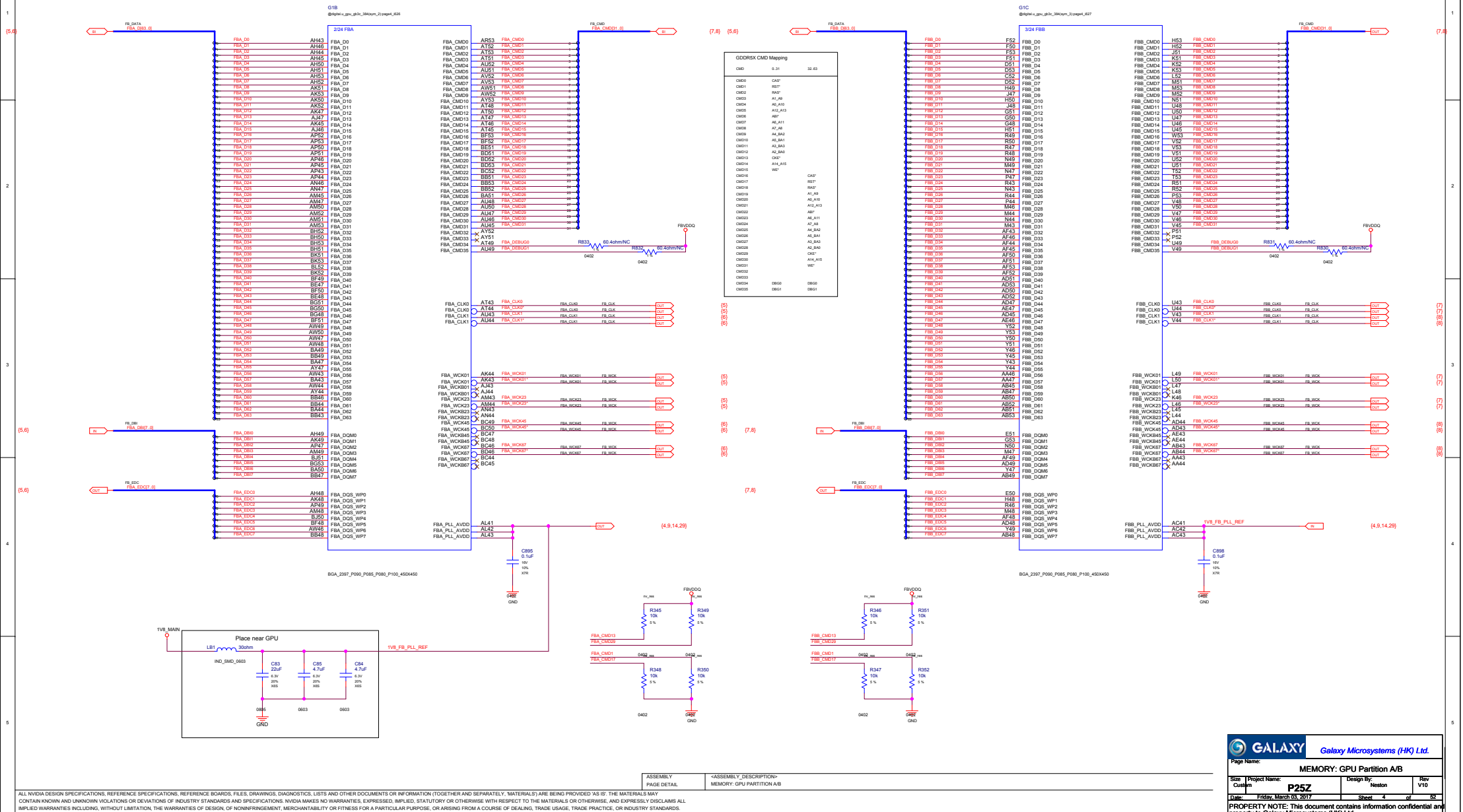
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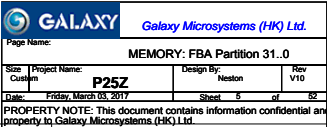
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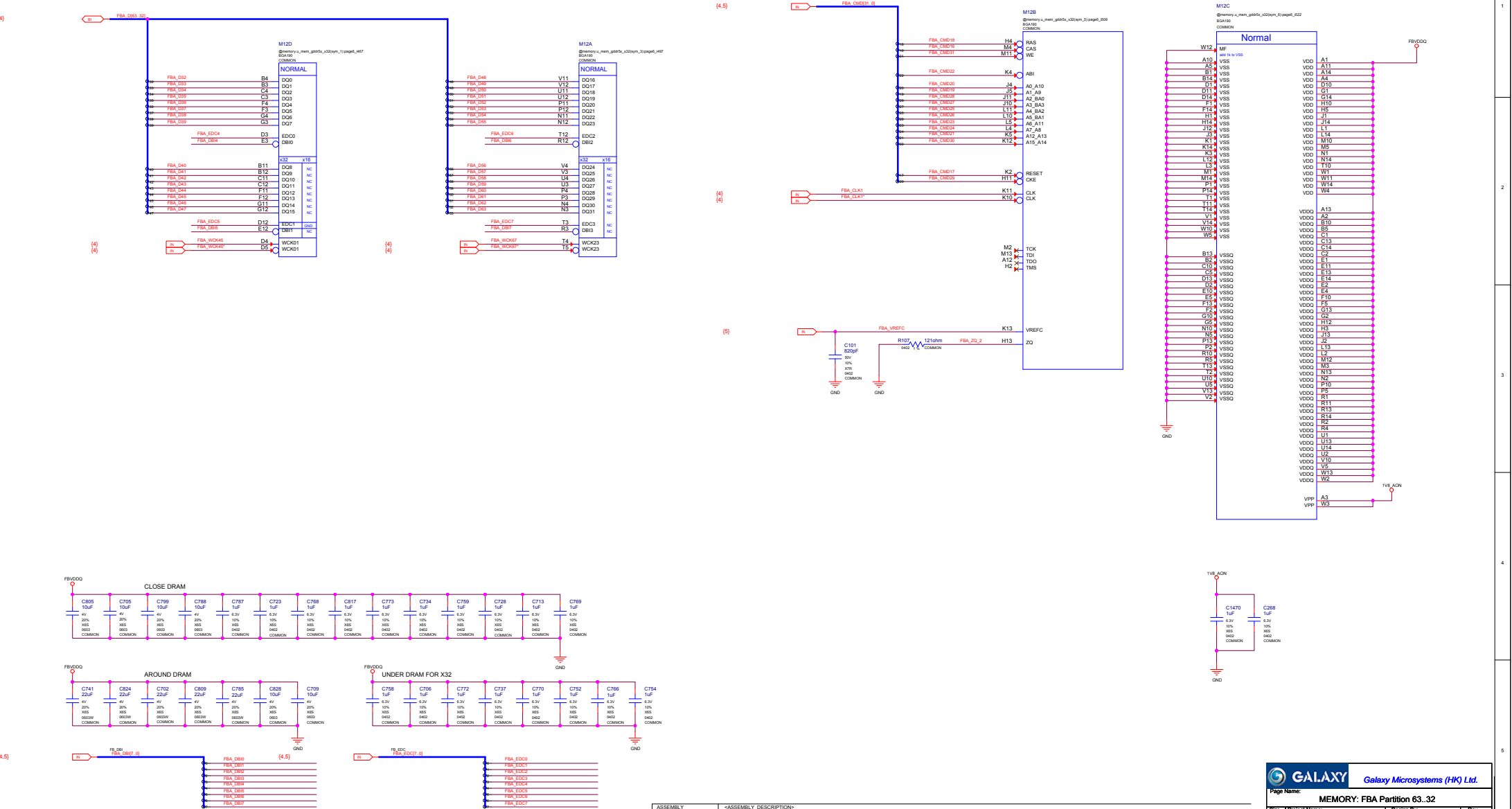
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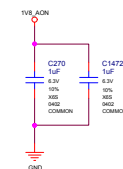
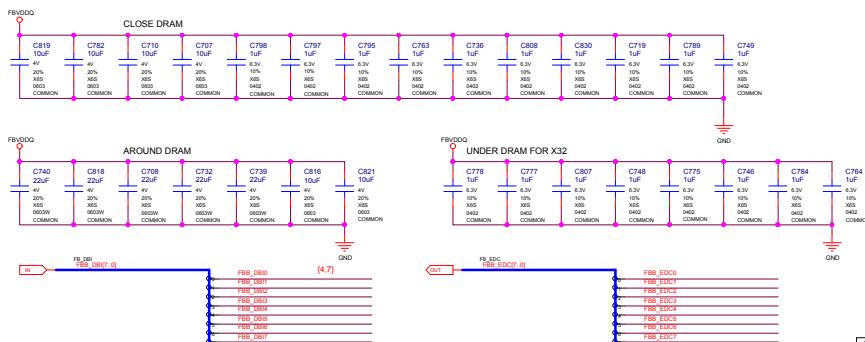
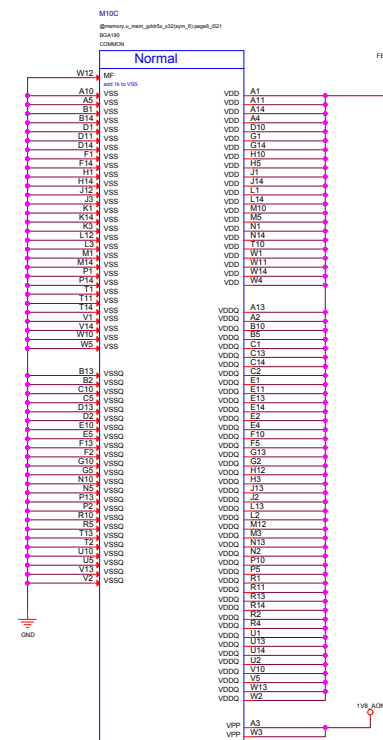
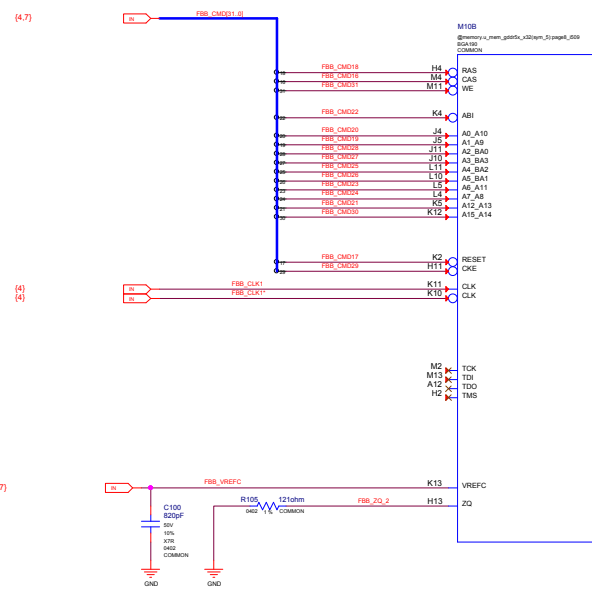
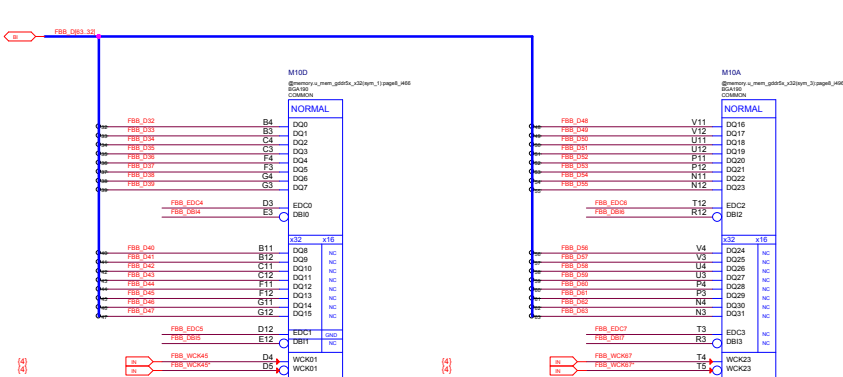
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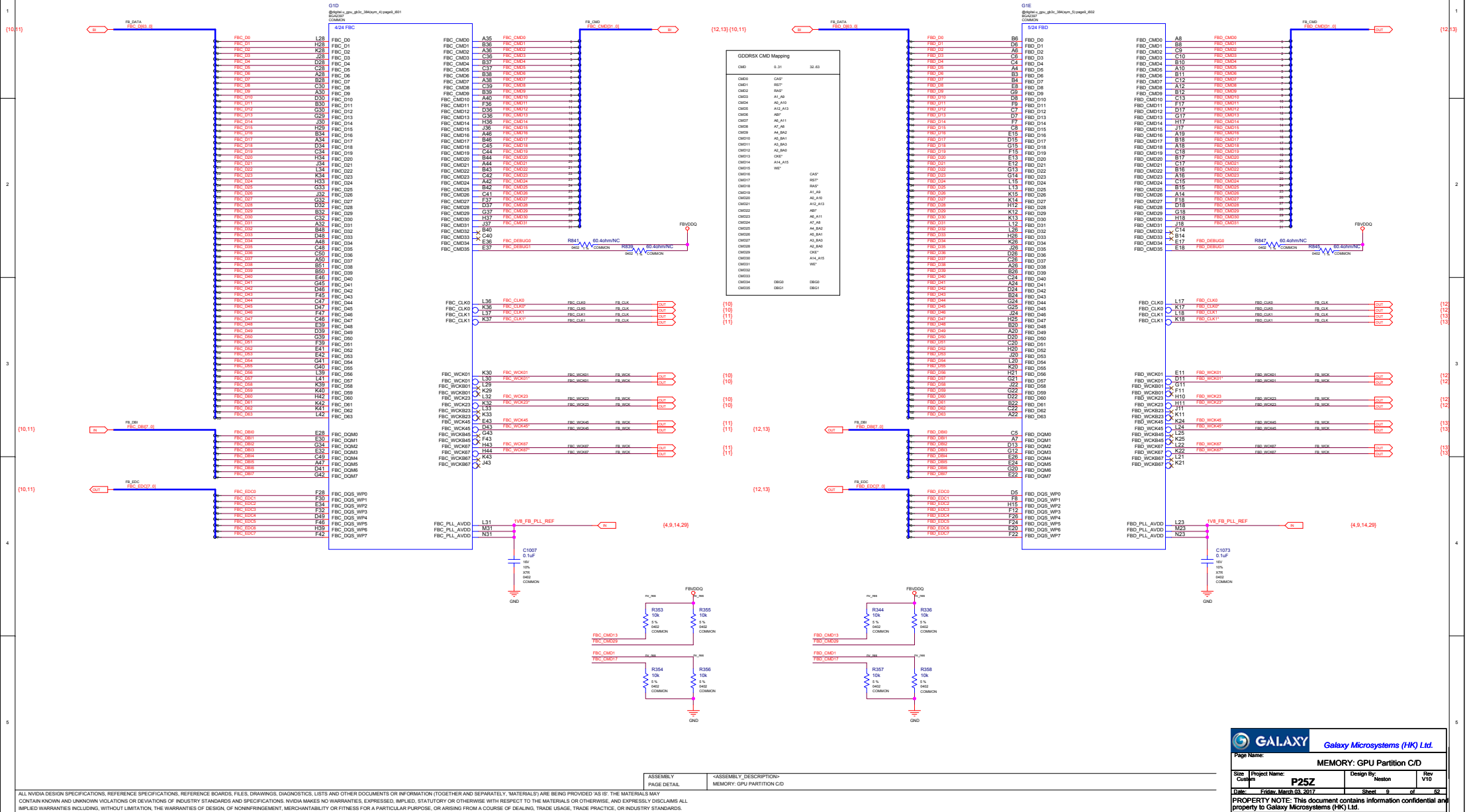


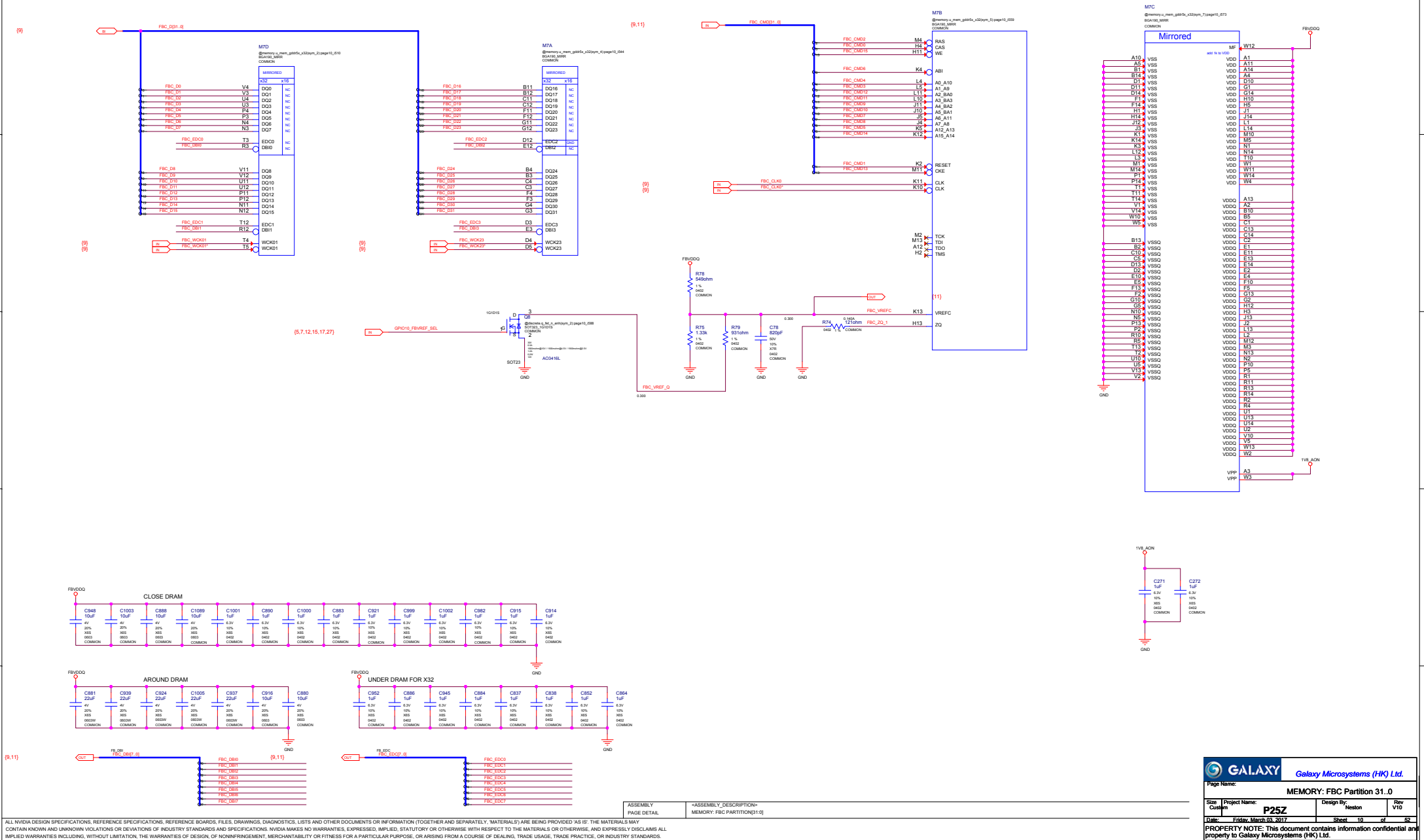
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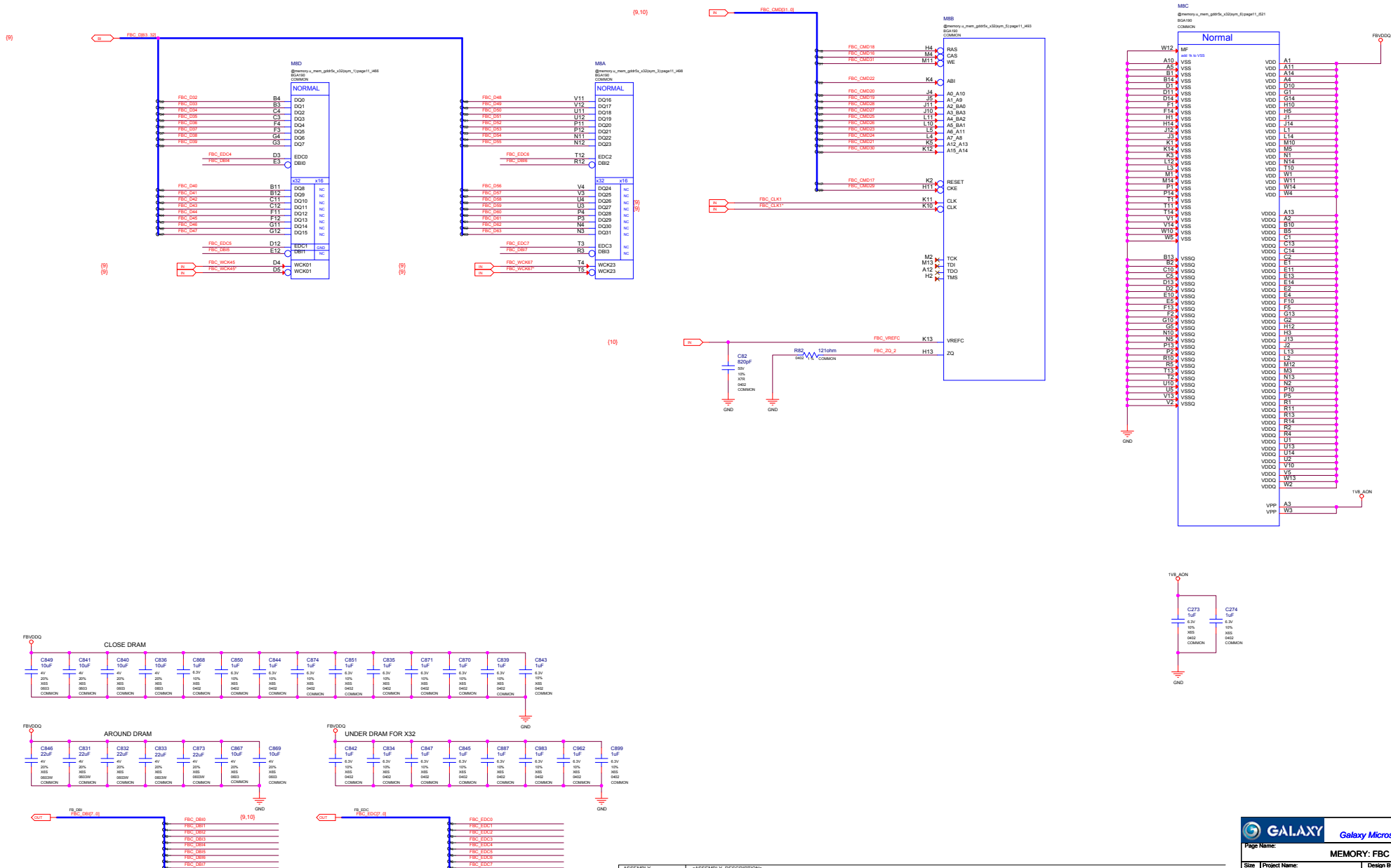


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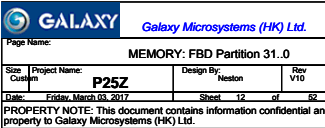
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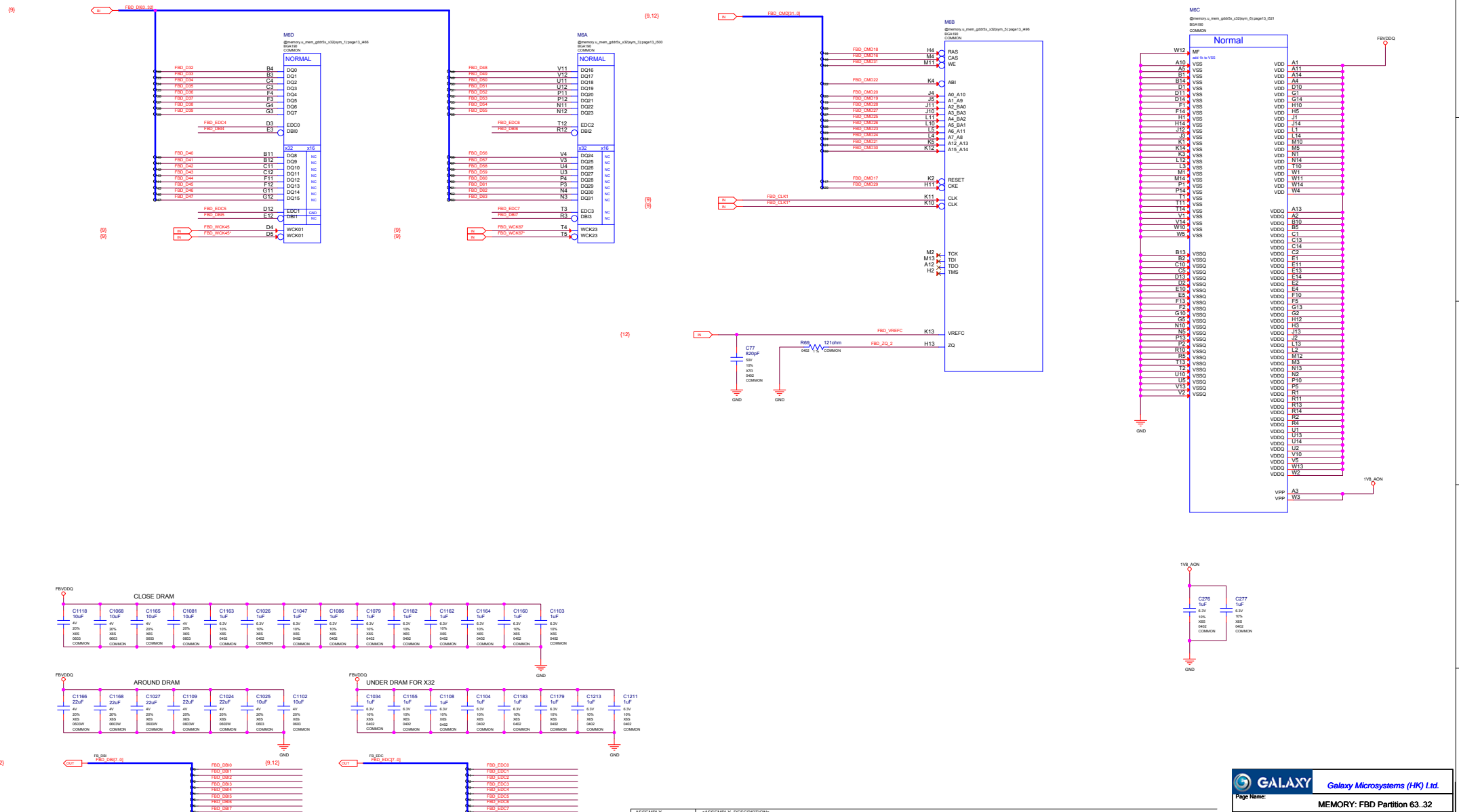




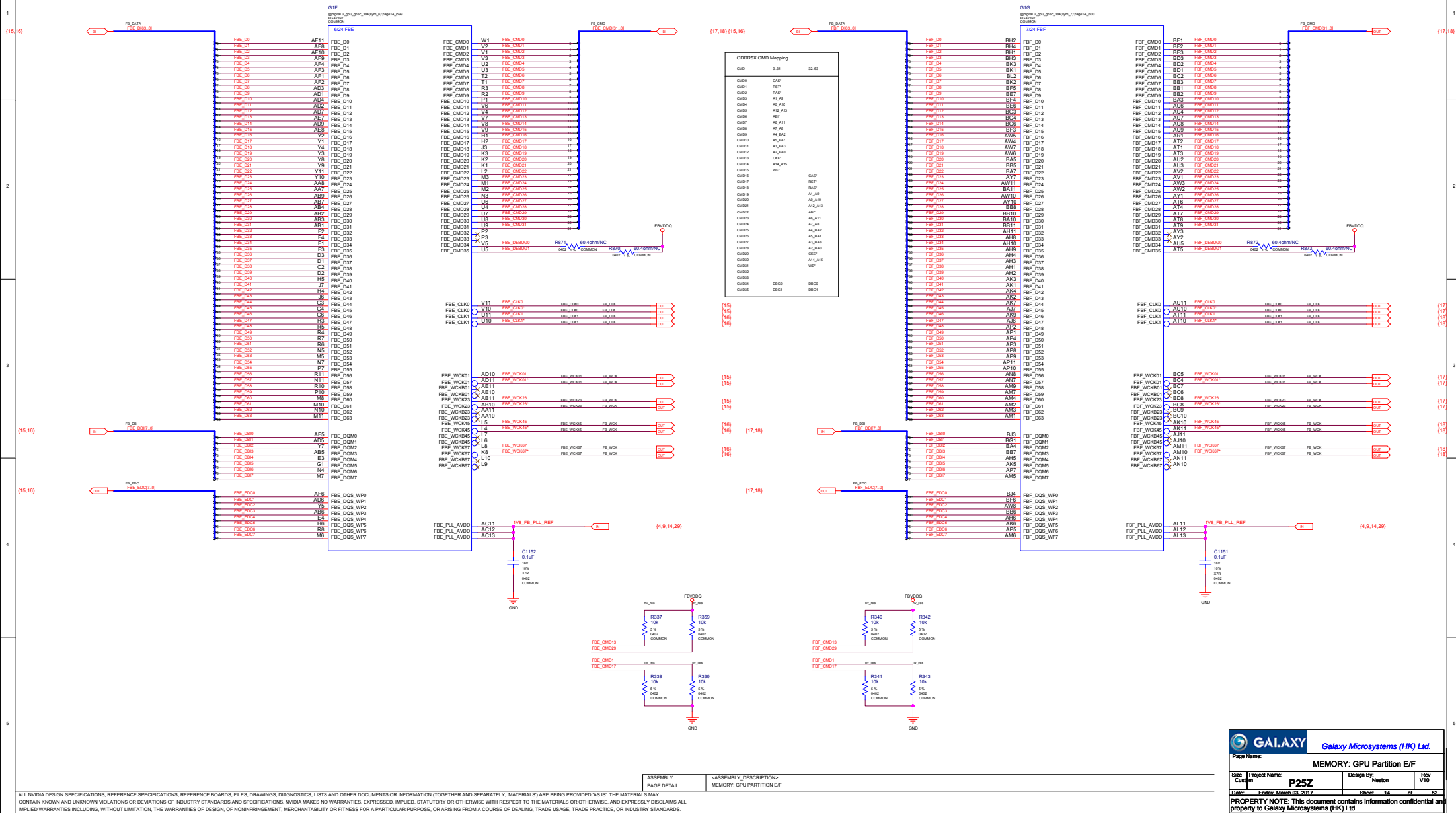


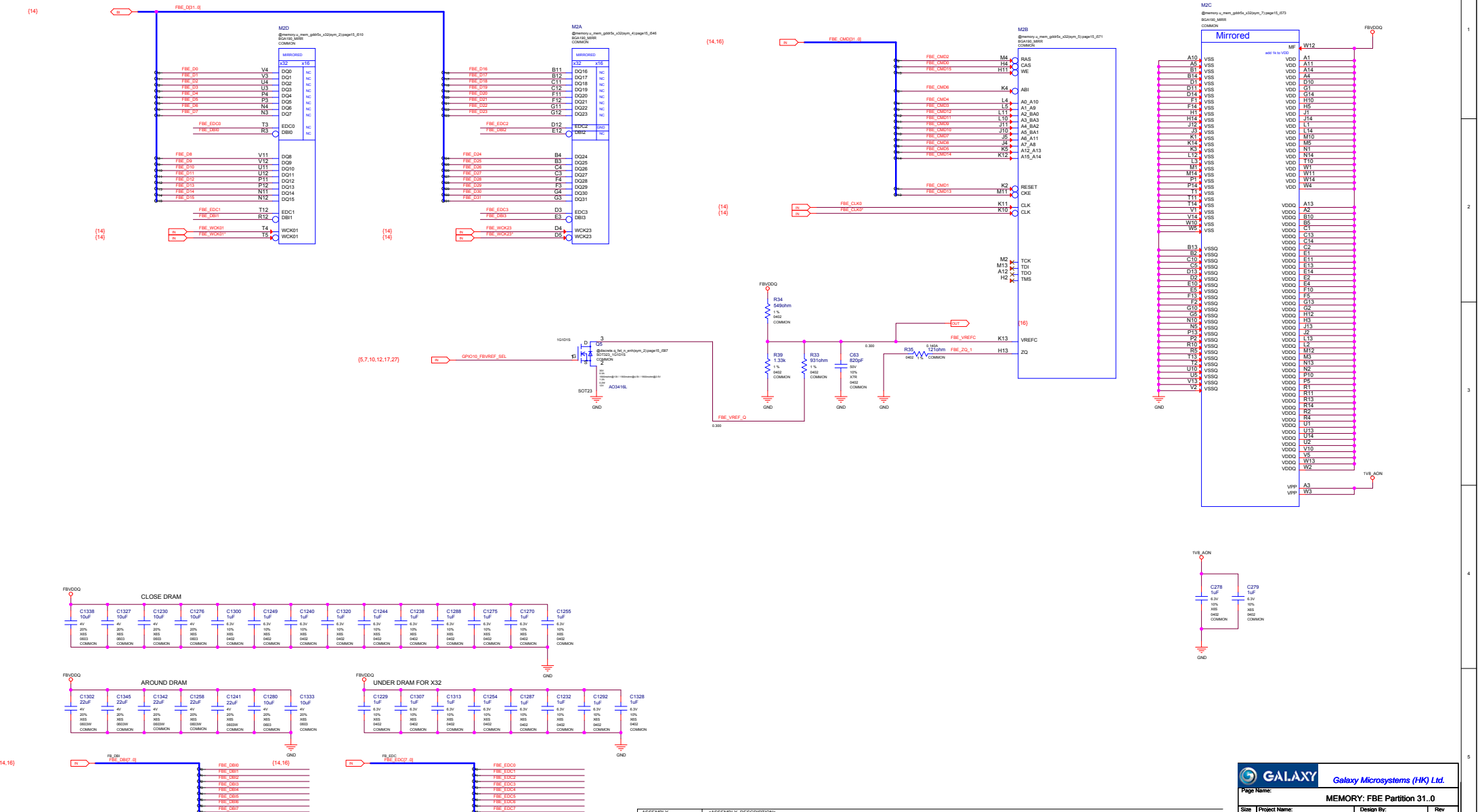
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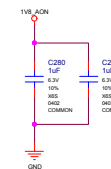
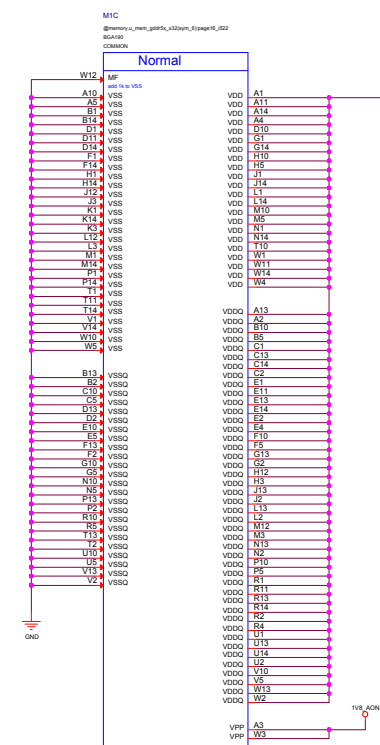
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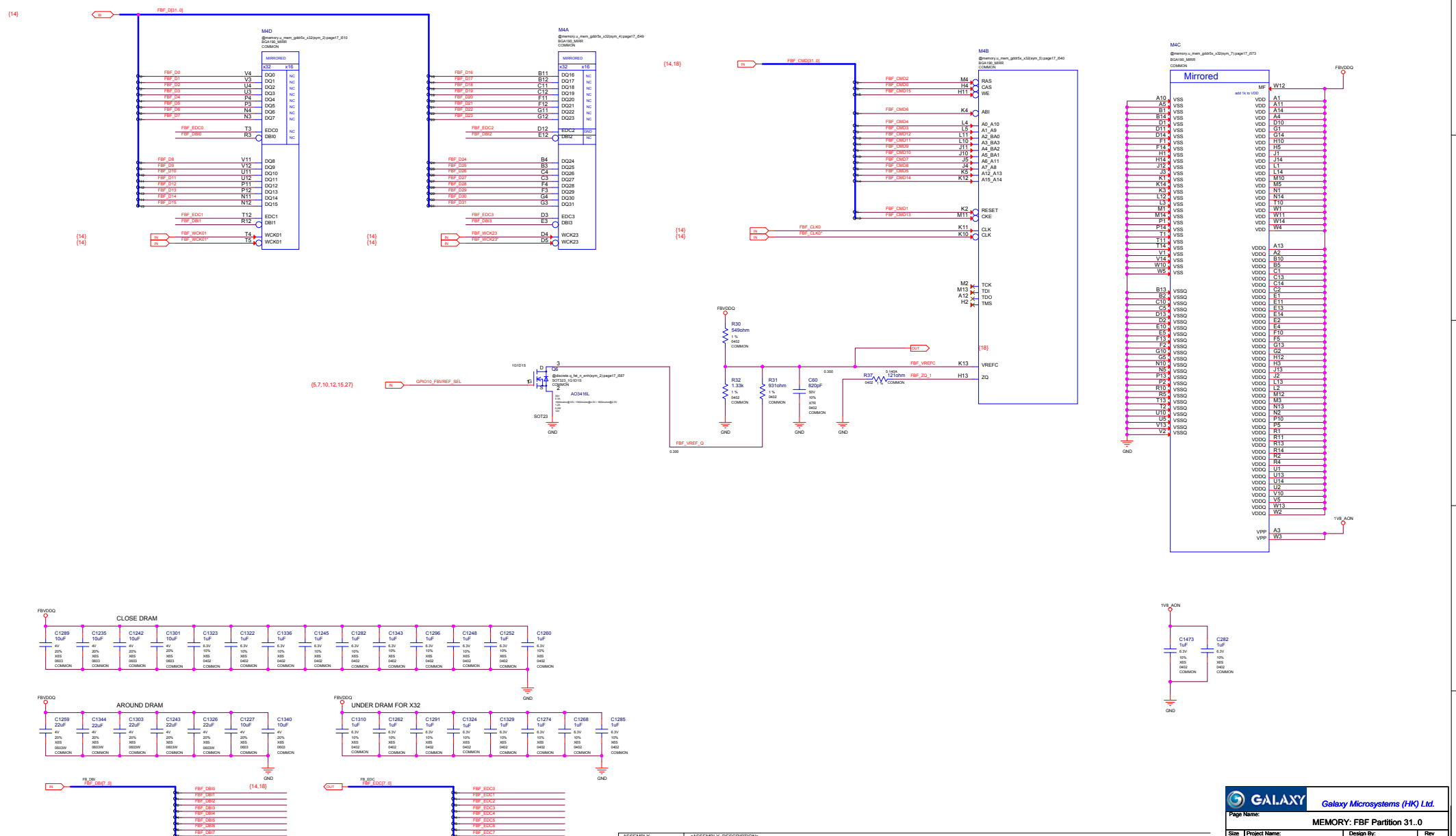
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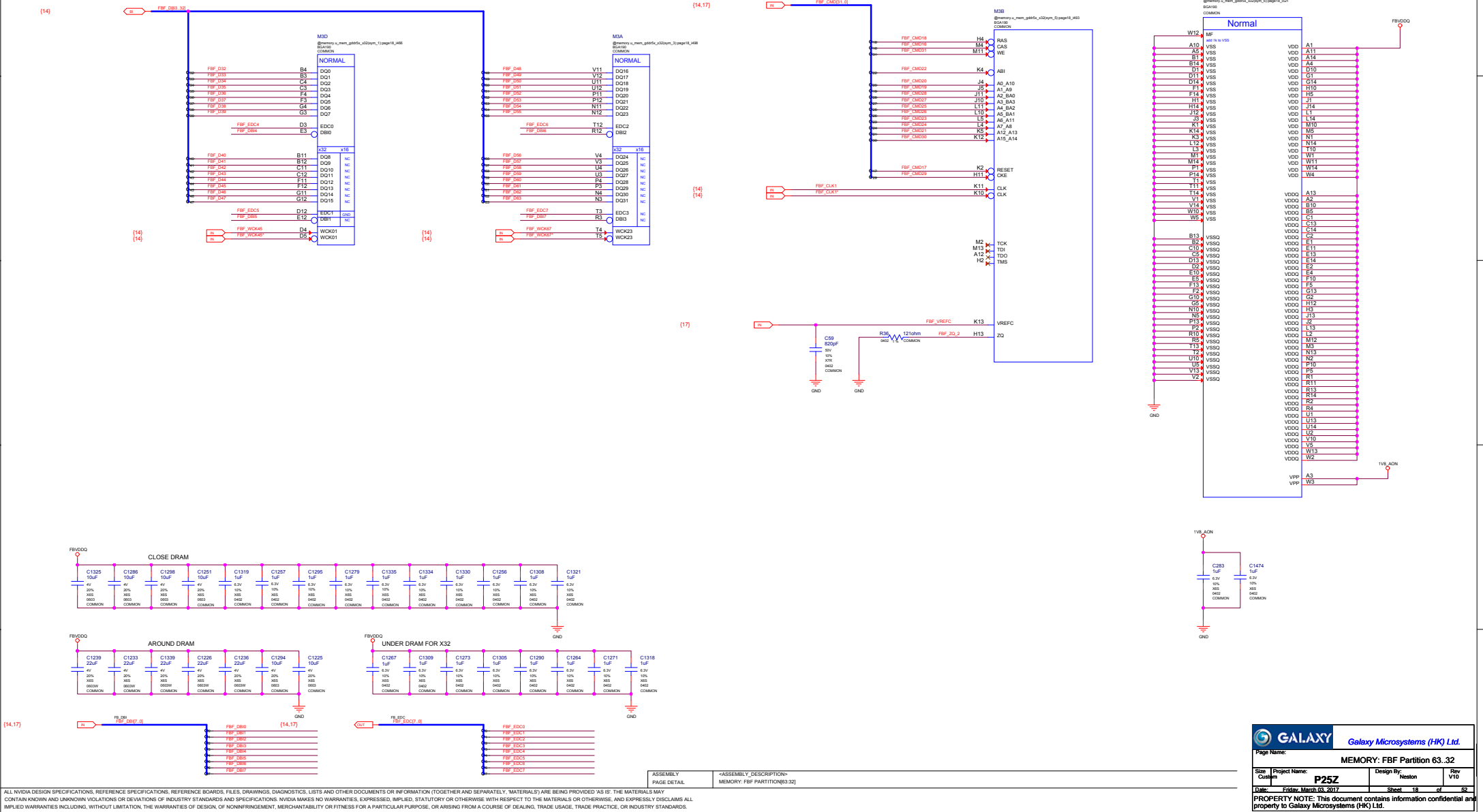
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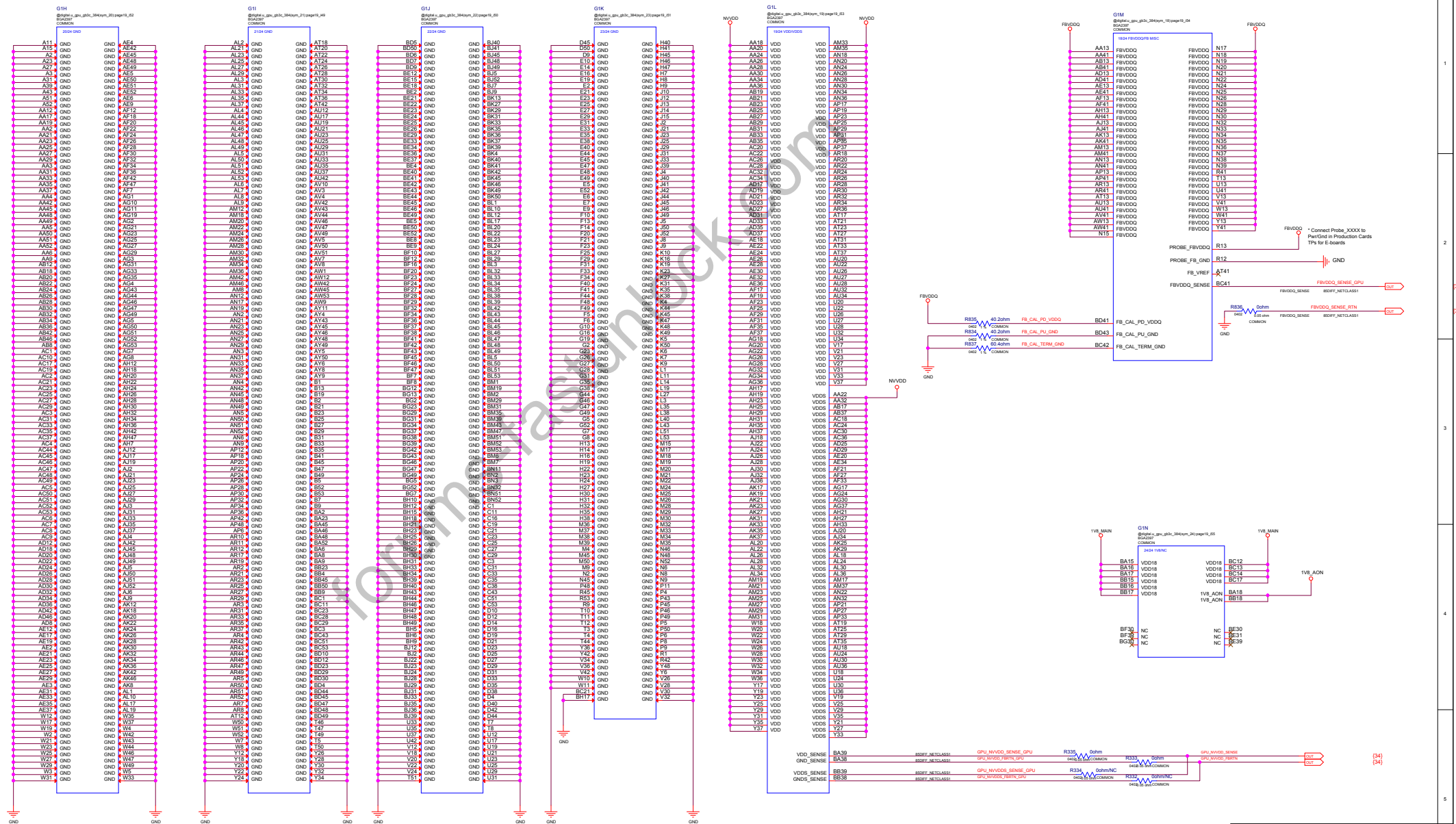
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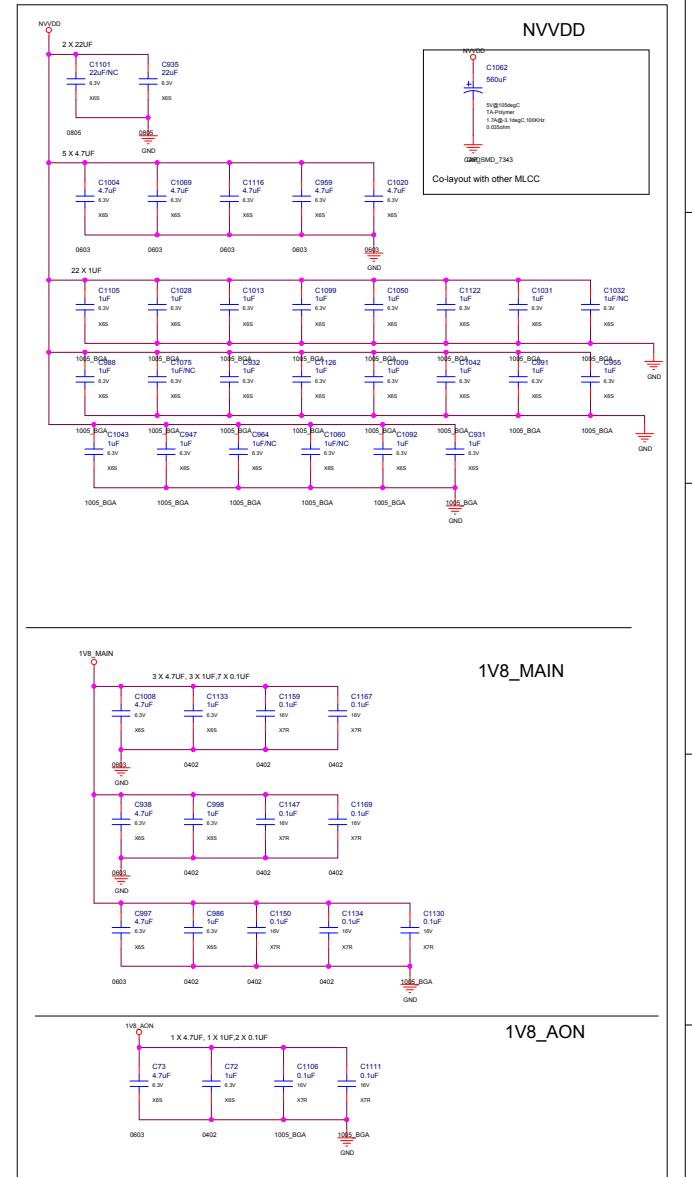
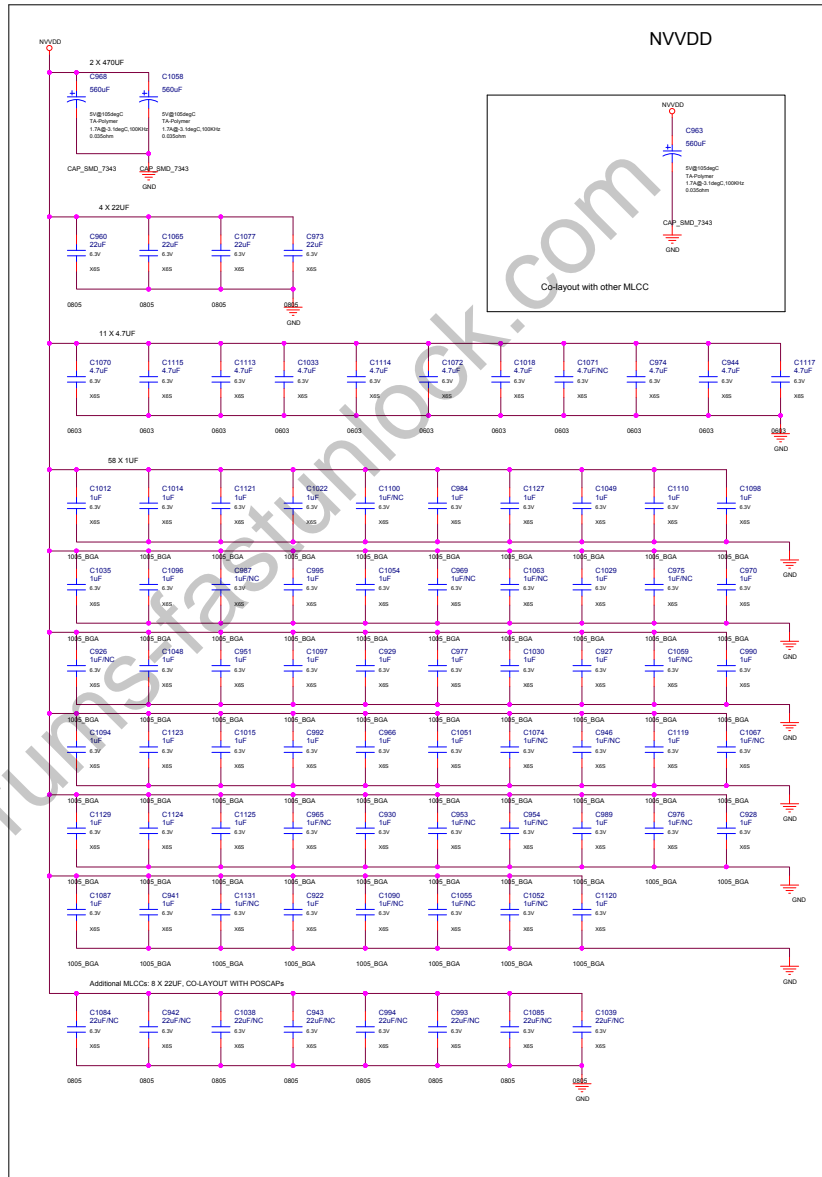
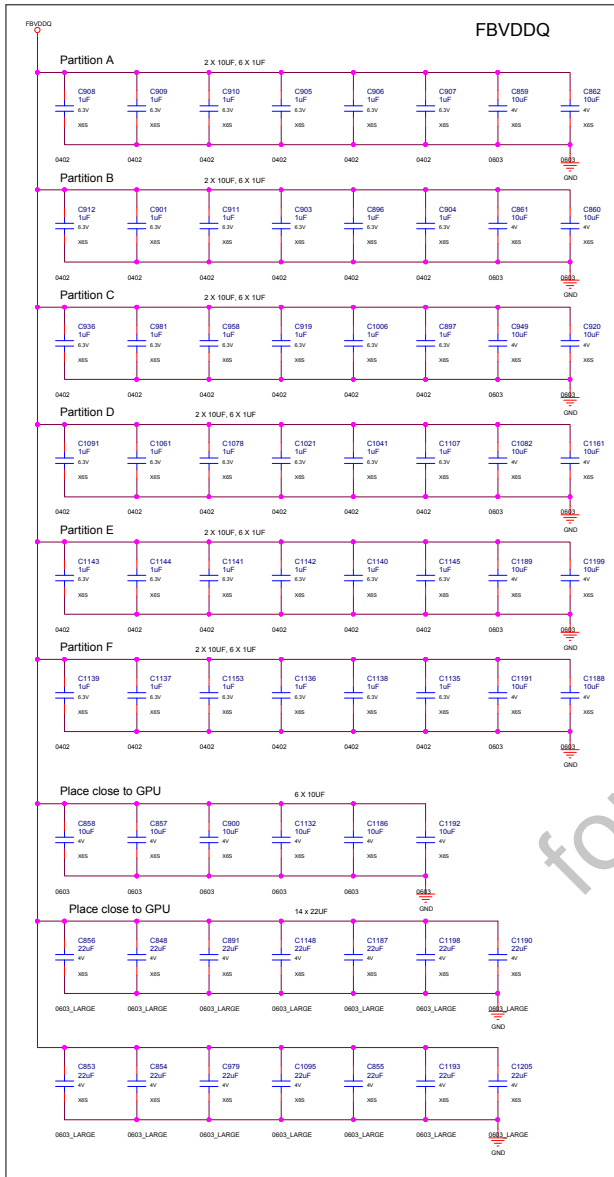
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PAGE DETAIL	GPU PWR AND GND

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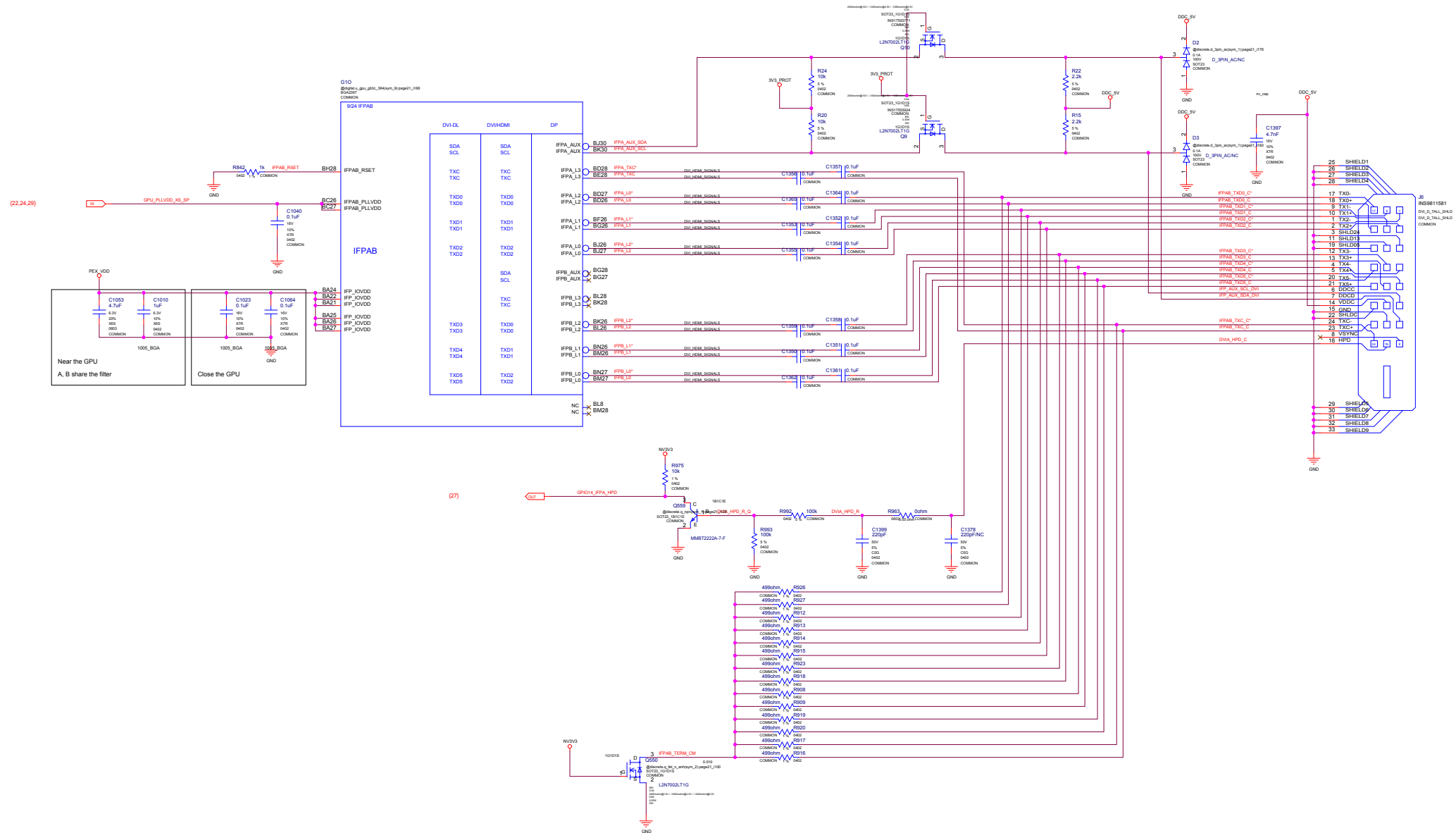
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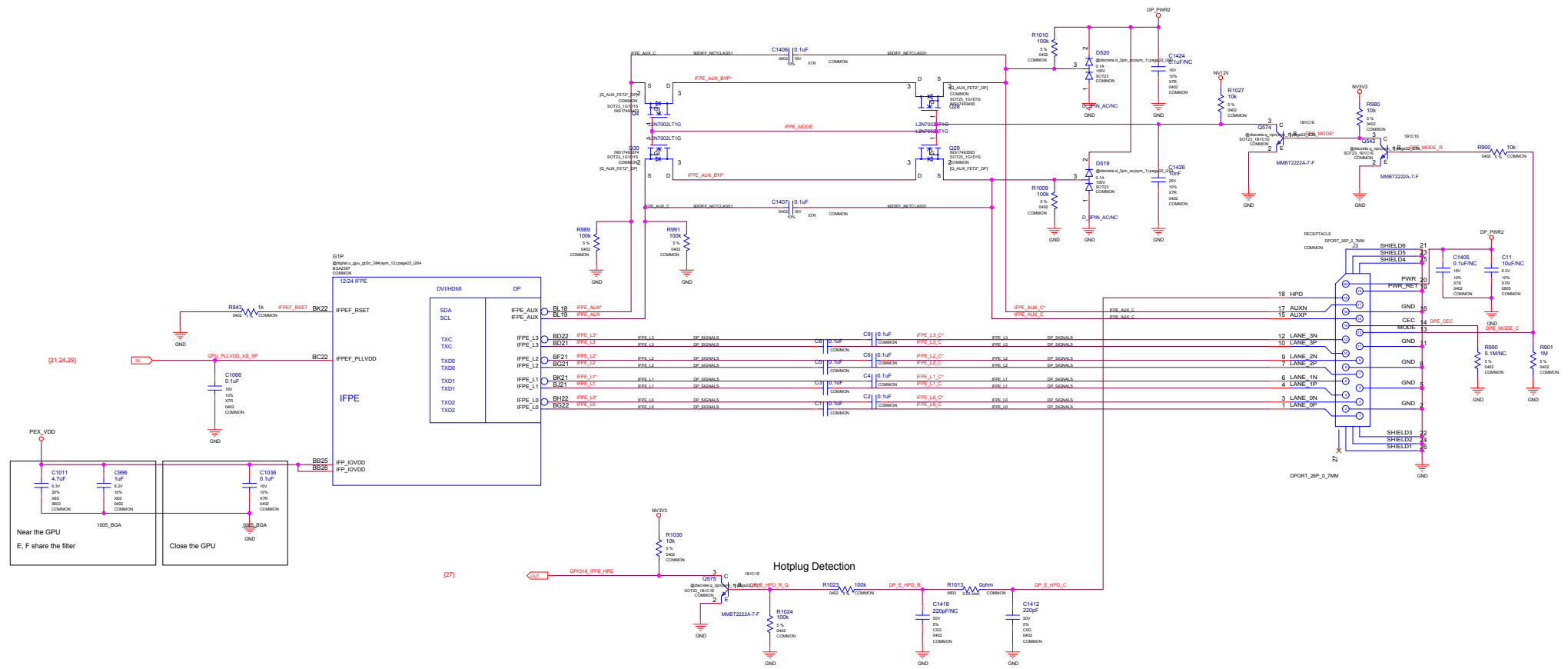
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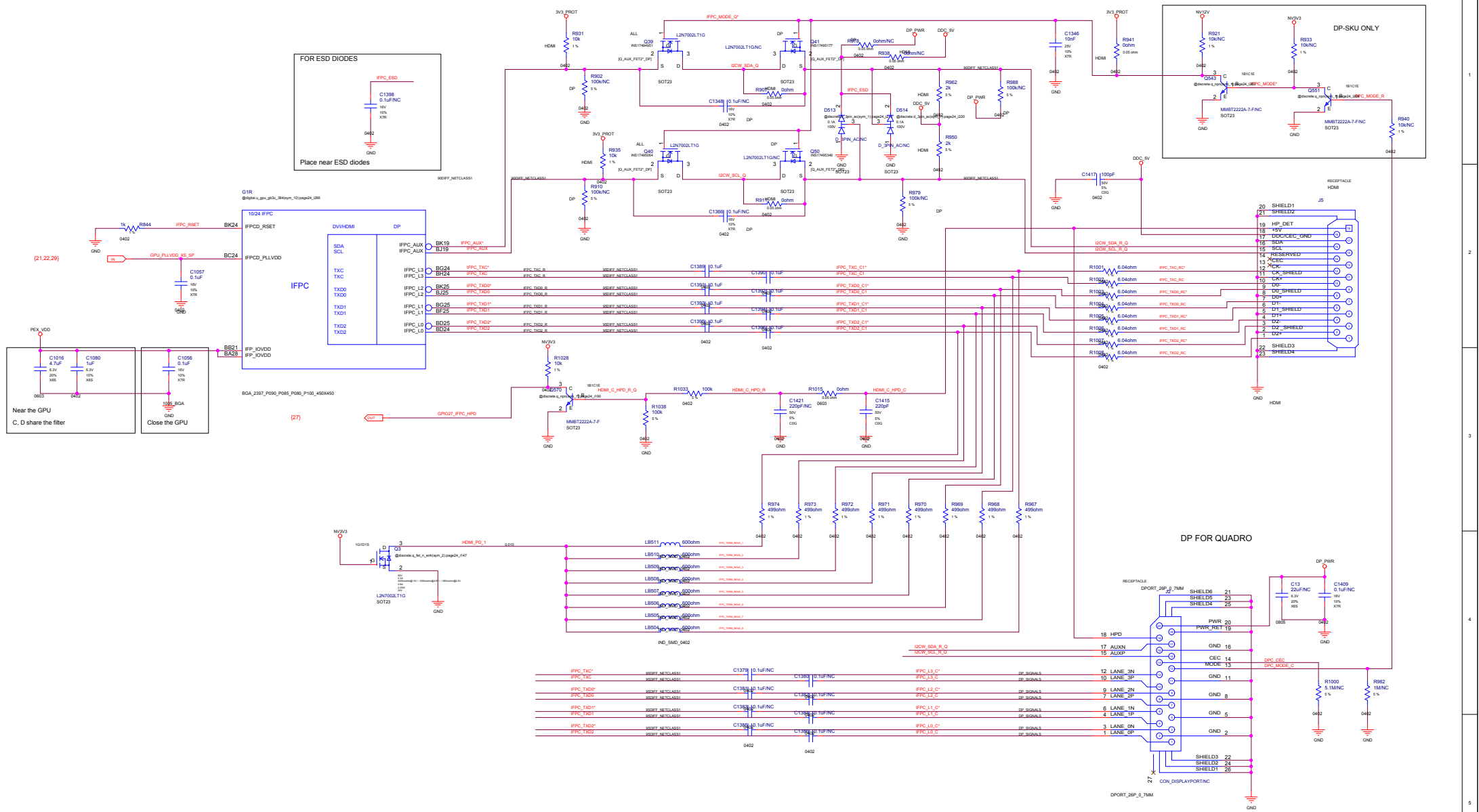
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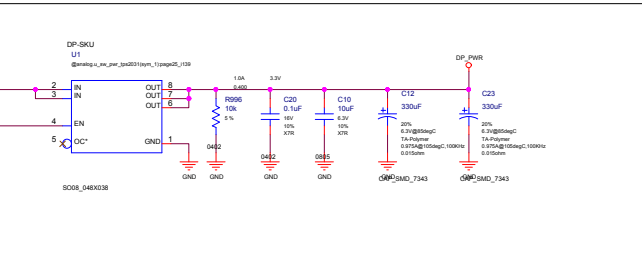
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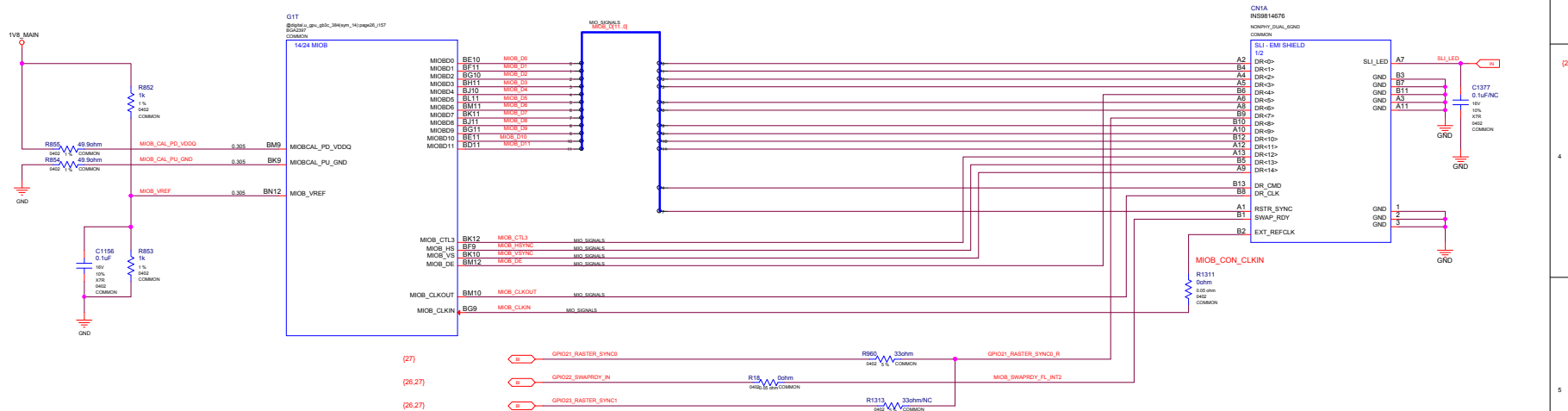
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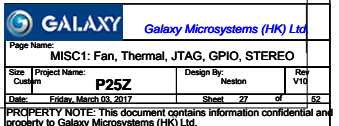


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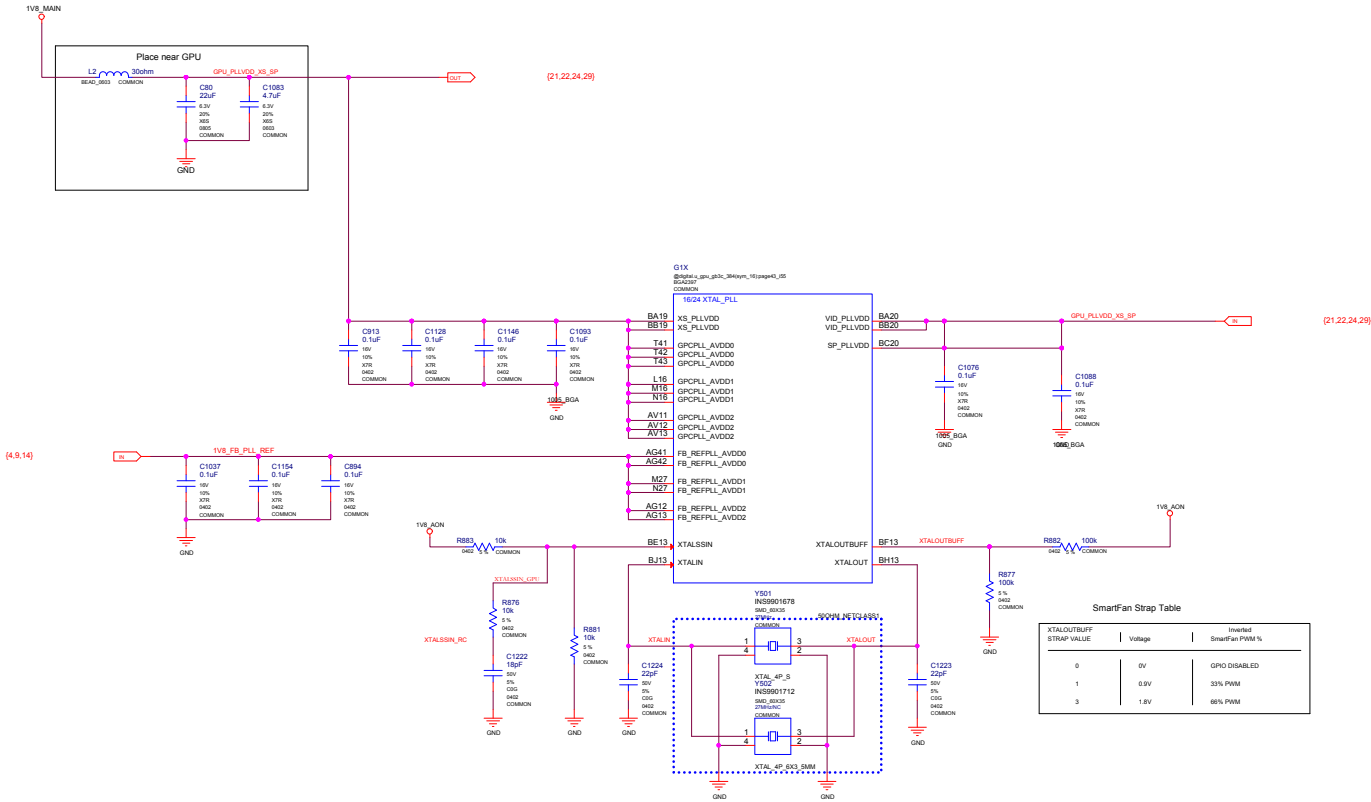


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0:PCIE_CFG HIGH POWER

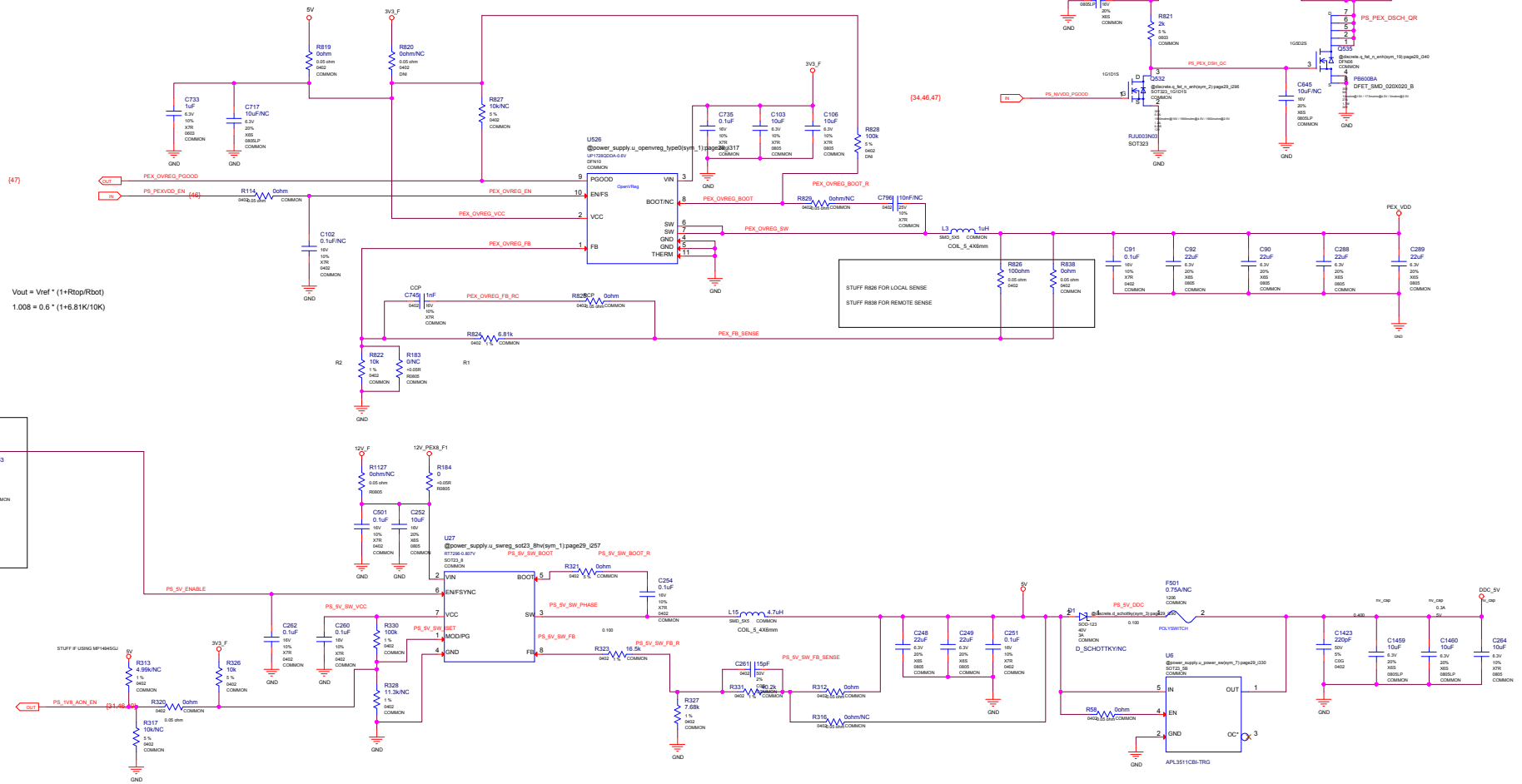
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
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PEX PLL Switcher

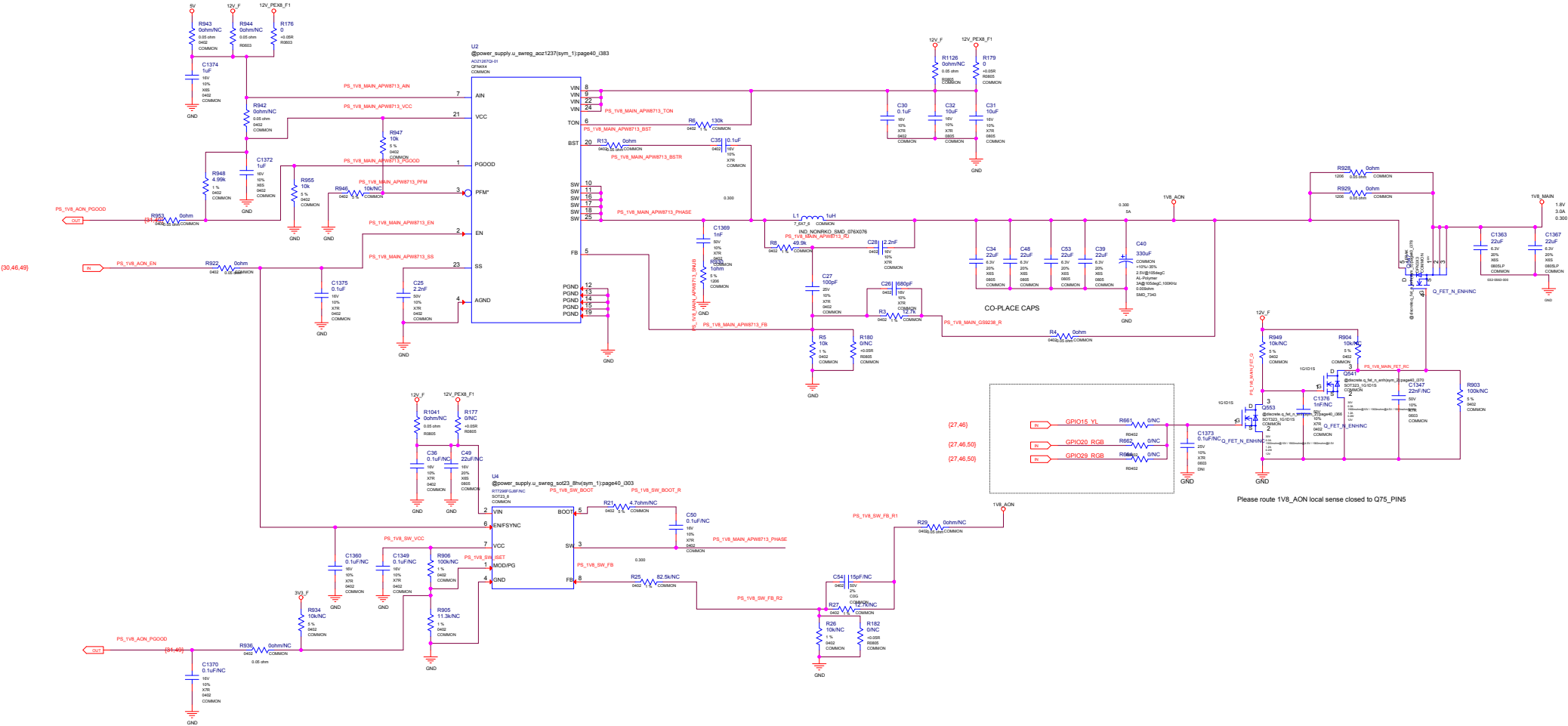


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 Galaxy Microsystems (HK) Ltd.			
Page Name:		PS: 5V, PEX_VDD	
Size	Project Name:	Design By:	Rev
Custm	P252	Neston	V10
Date:	Friday, March 03, 2017	Sheet	30 of 52
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$$1.8 = 0.5 * (1 + 18.7K/15K)$$
$$V_{out} = V_{ref} * (1 + R_{top}/R_{bot})$$

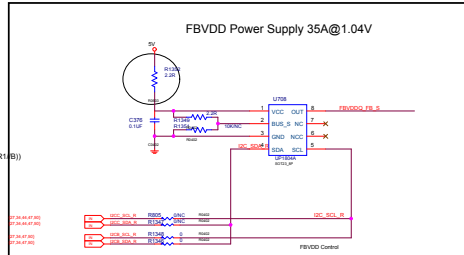
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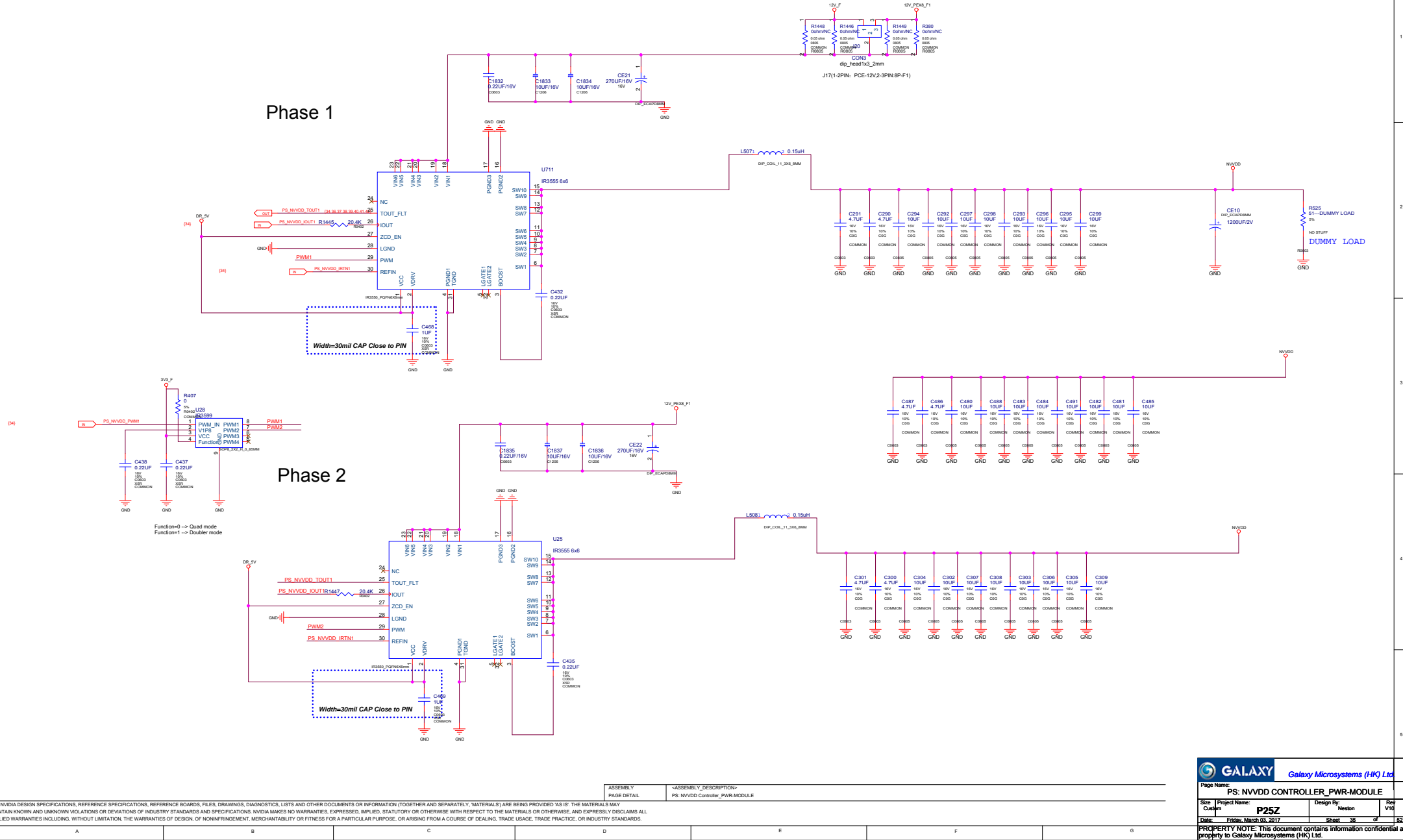
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PAGE DETAIL	PS: 1V8 Rails

Page Name: **PS: 1V8 Rails**

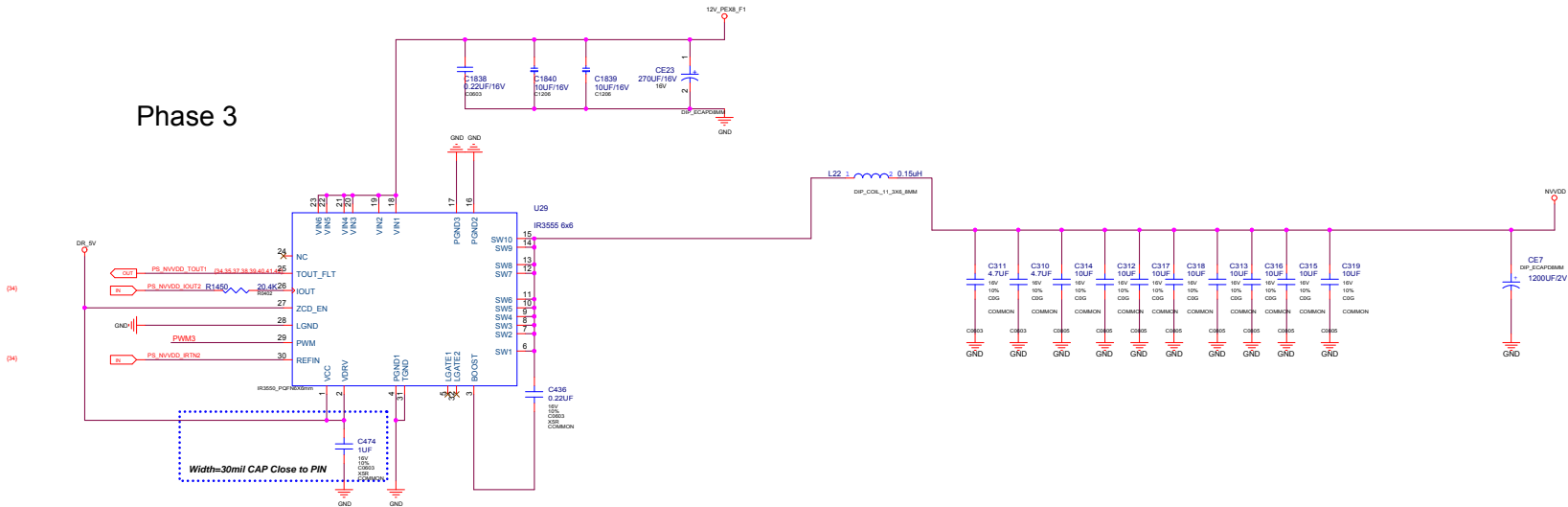
Size	Project Name:	Design By:	Rev
Cu/In	P25Z	Heston	V1.0
Date:	Friday, March 08, 2017	Sheet	31 of 82

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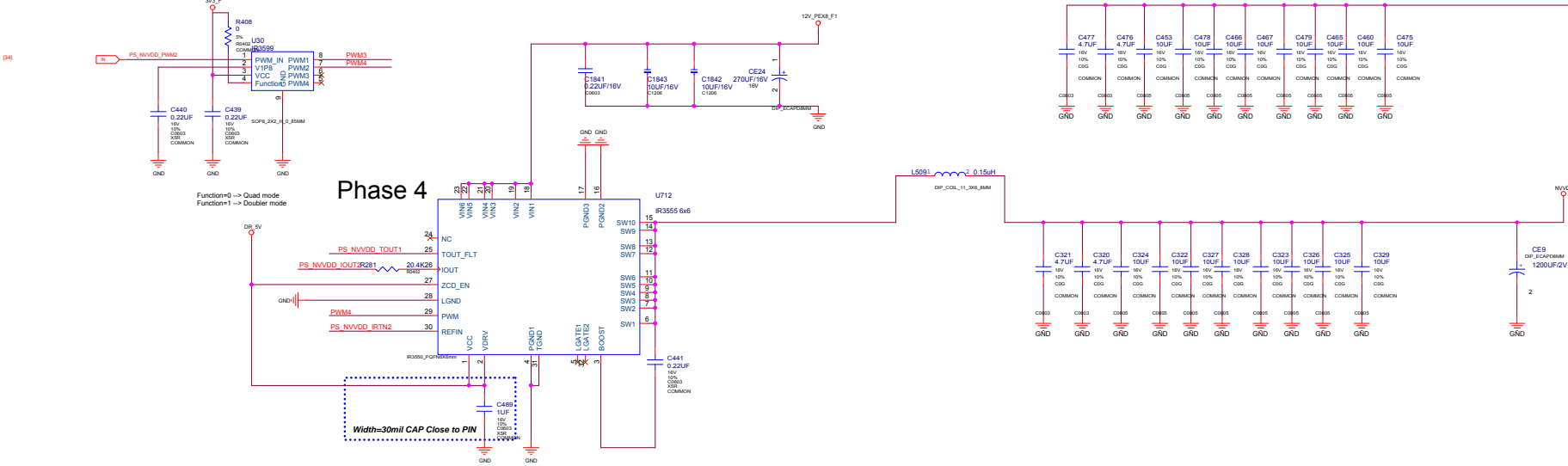





Phase 3



Phase 4



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Page Name:

PS: NVVDD Phase 1,2

Size

Project Name:

Design By:

Rev

Cu

P25Z

Heston

V1.0

Date:

Sheet

of

82

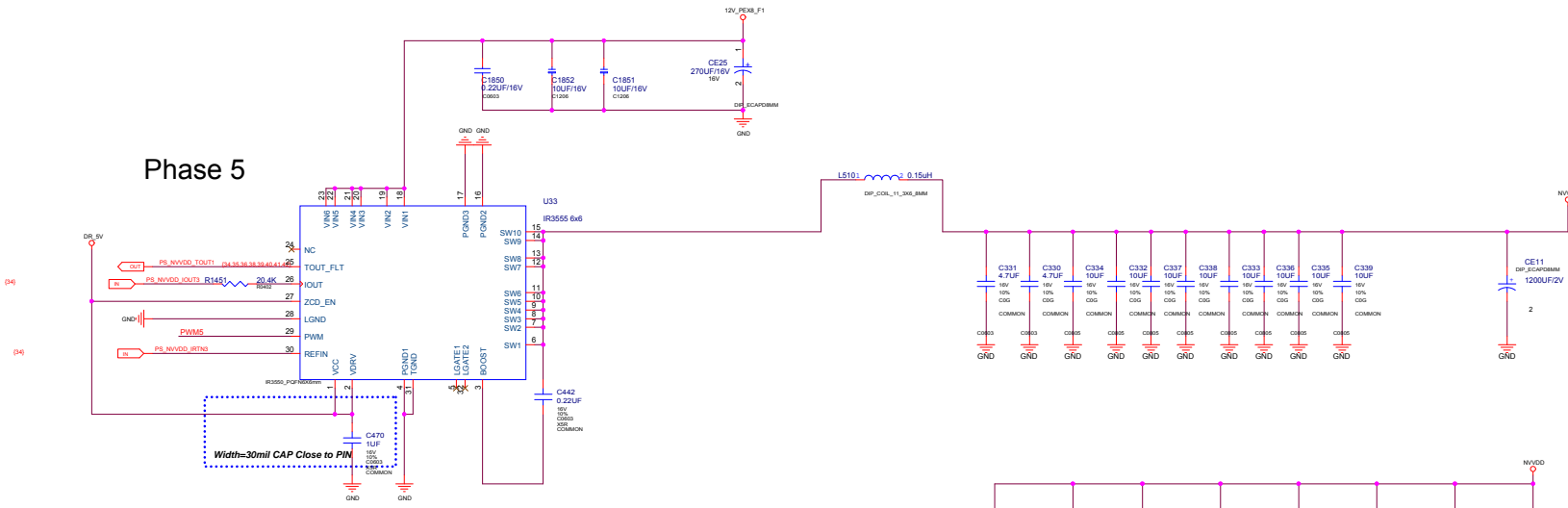
Friday, March 03, 2017

38

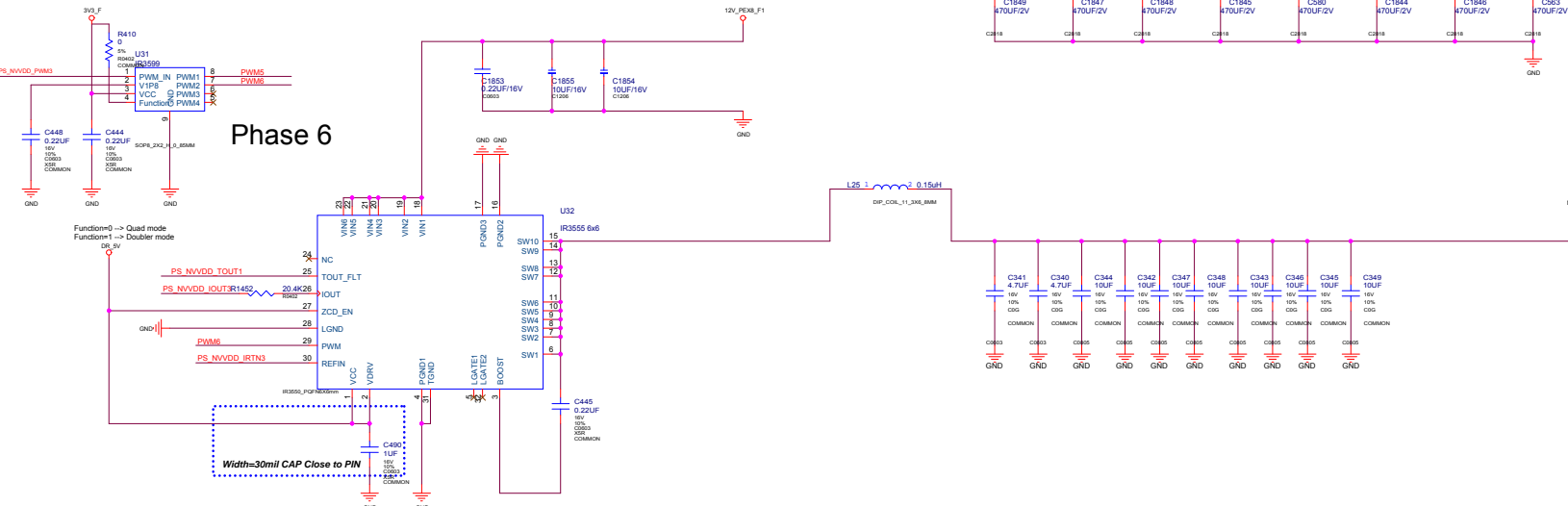
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Phase 5



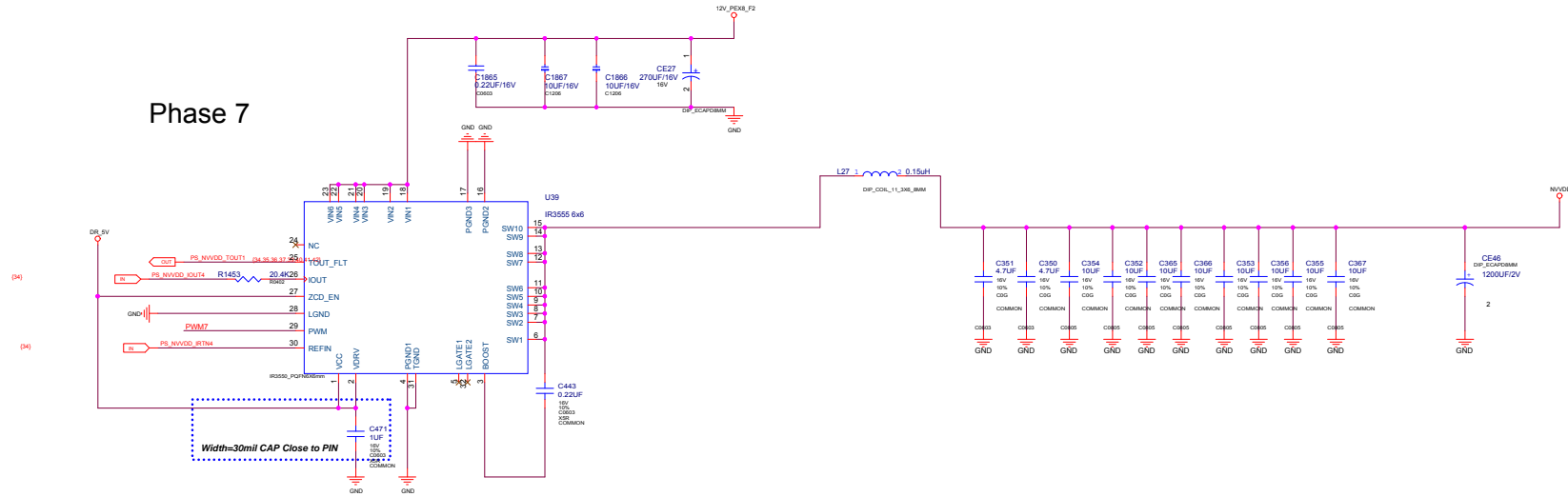
Phase 6



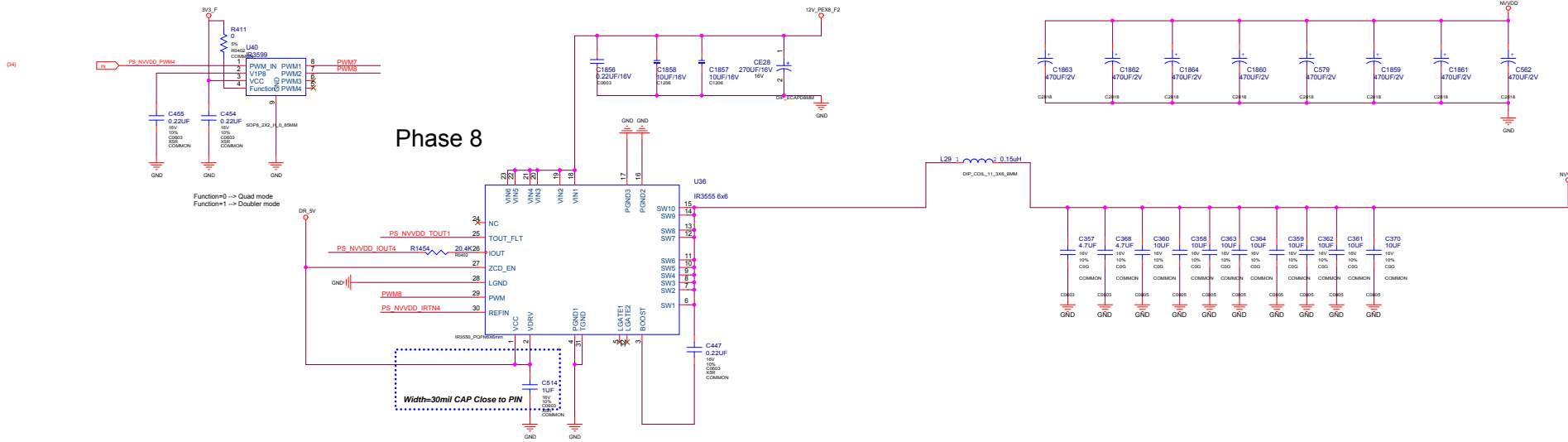
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Page Name: PS: NVVDD Phase 3,4			
Size	Project Name: P25Z	Design By: Heston	Rev: V1.0
Customer	Date: Friday, March 03, 2017	Sheet: 37	of 82
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Phase 7



Phase 8



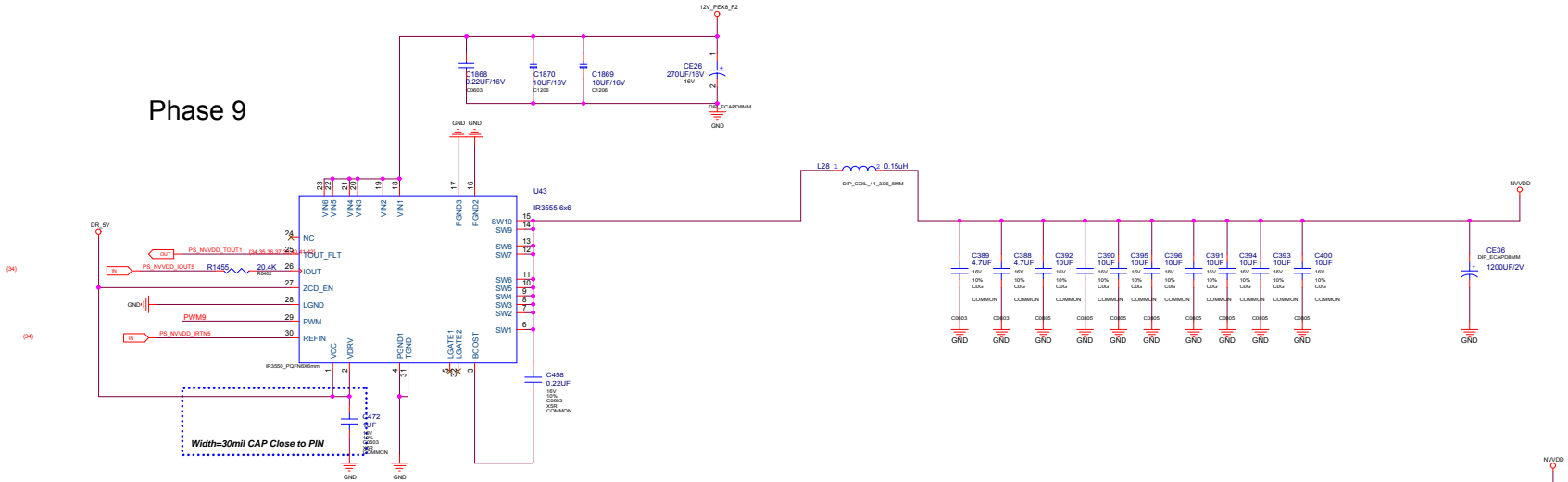
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ASSEMBLY
PAGE DETAIL

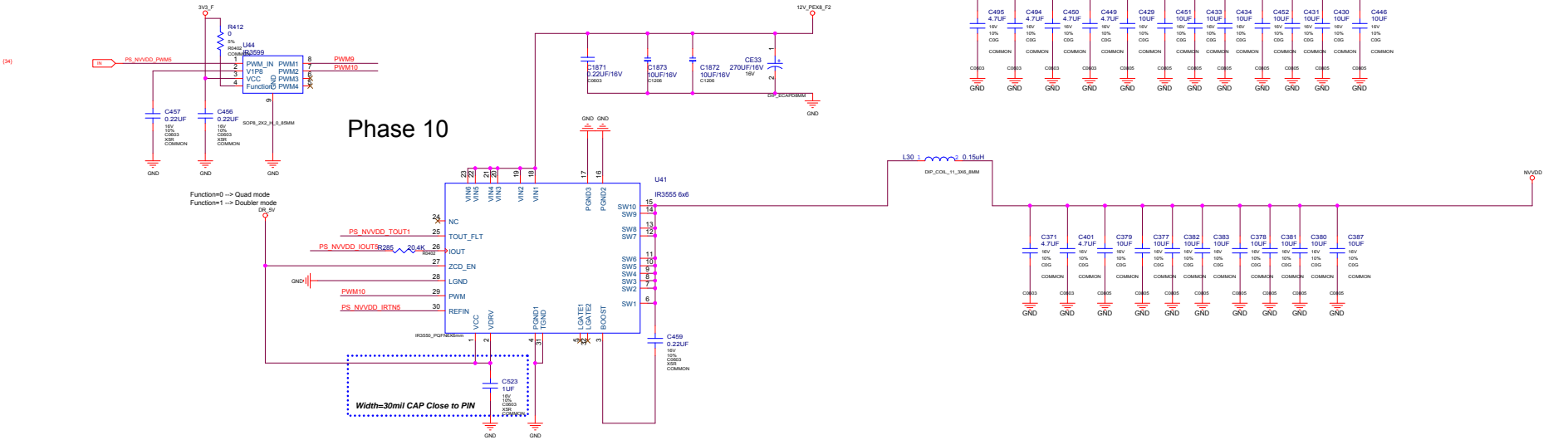
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Page Name: PS: NVVDD Phase 5			
Size: Cus001	Project Name: P25Z	Design By: Heston	Rev: V1.0
Date: Friday, March 08, 2017	Sheet: 38	of 89	
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Phase 9



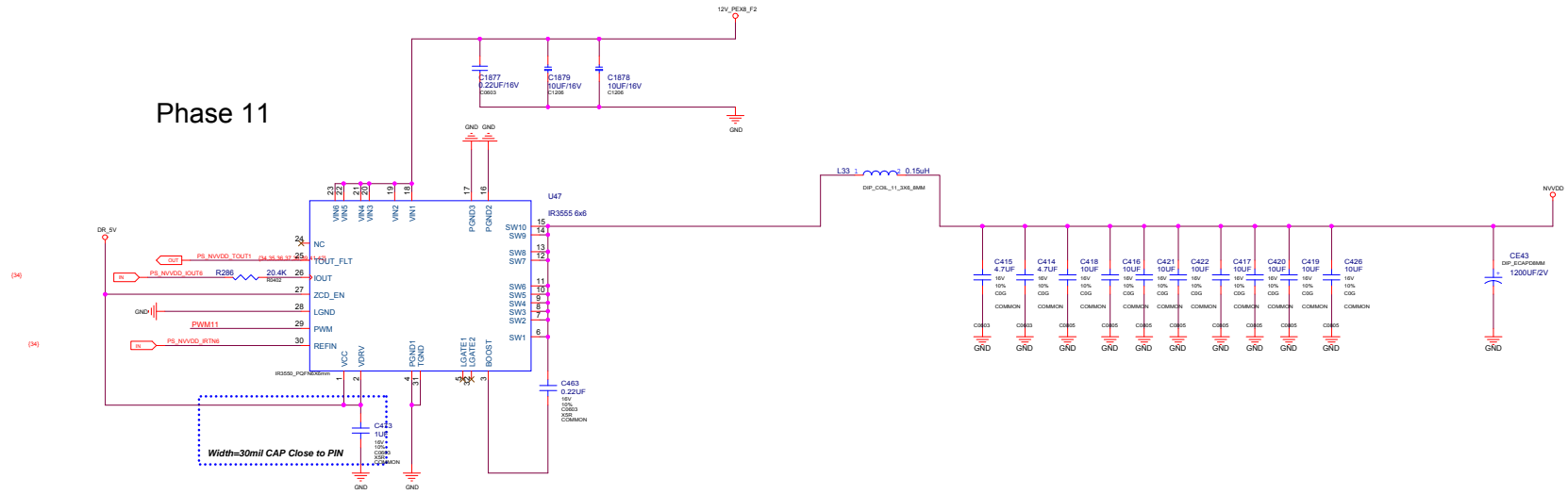
Phase 10



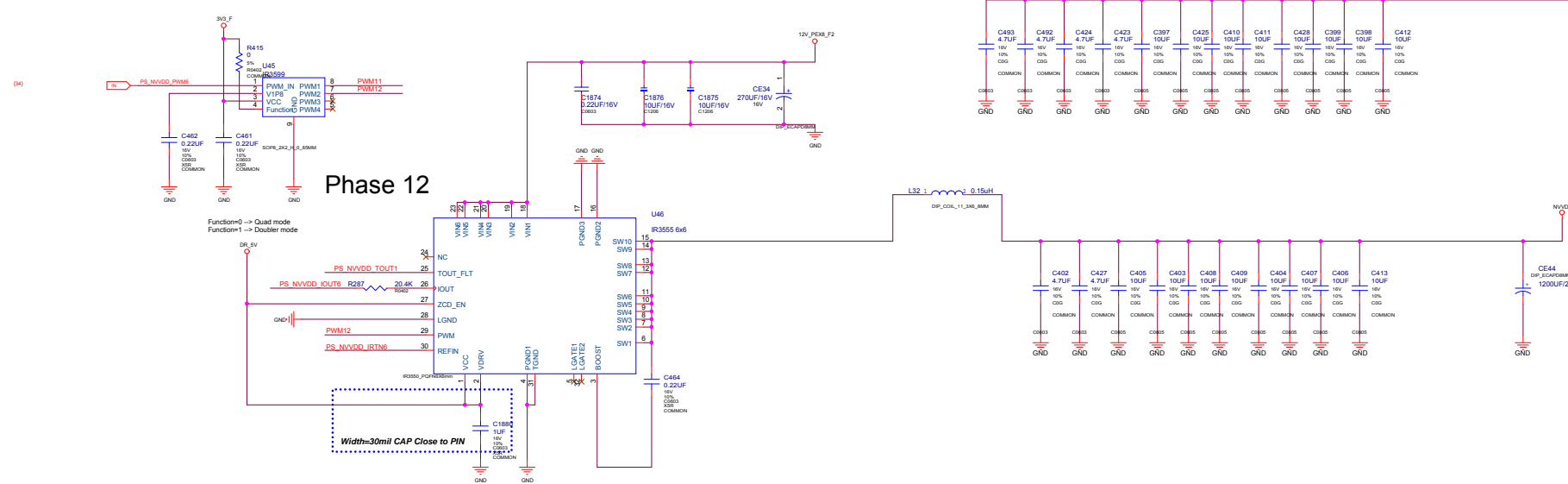
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Page Name: PS: NVVDD Phase 6,7			
Size: Cullen	Project Name: P25Z	Design By: Heston	Rev: V10
Date: Friday, March 03, 2017			
Sheet: 39 of 82			
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Phase 11



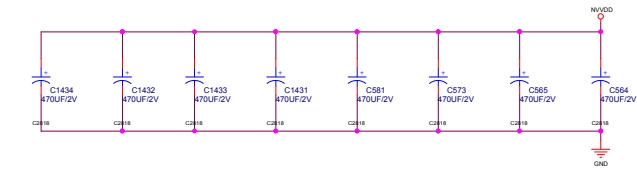
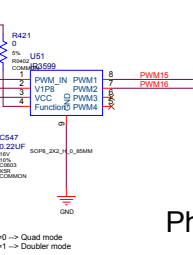
Phase 12

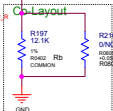


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Dynamic power balance phase

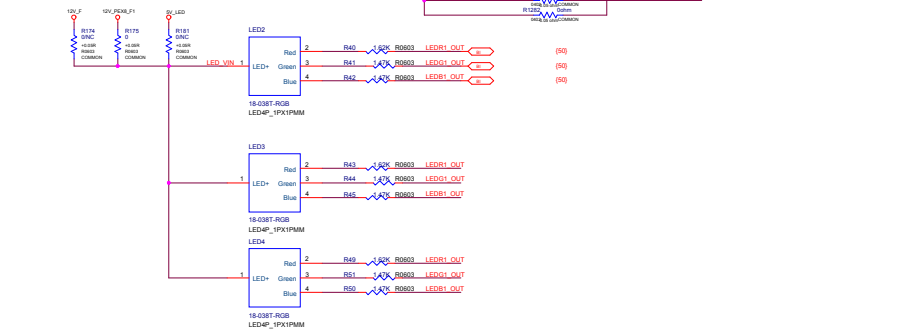
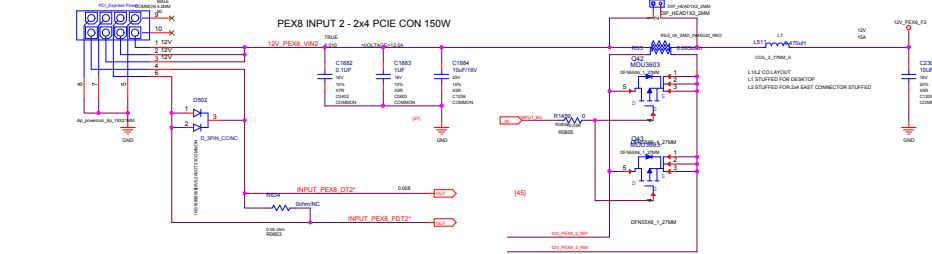
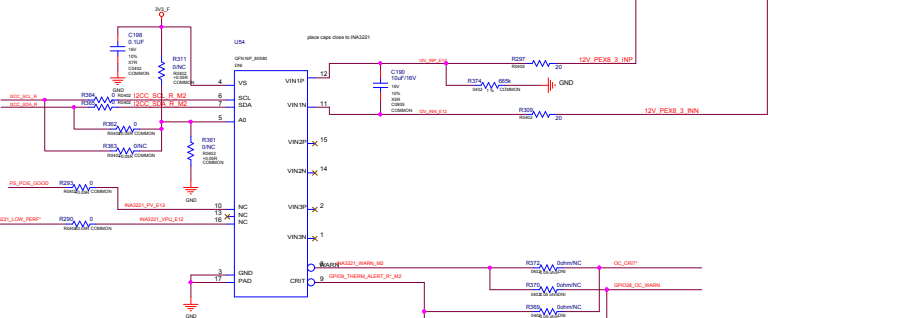
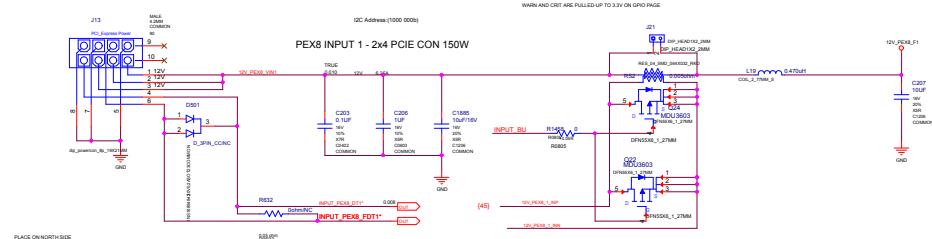
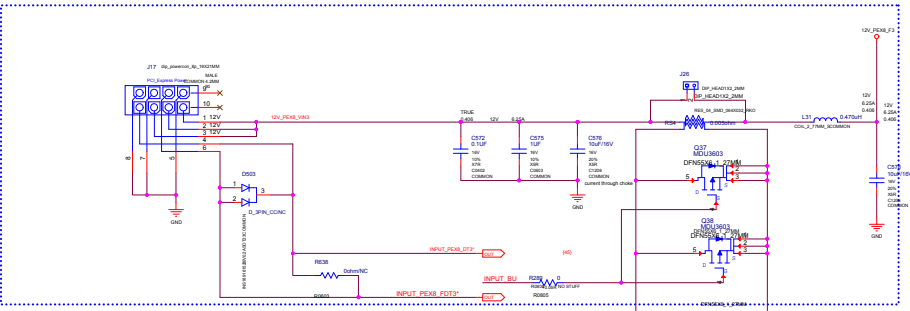
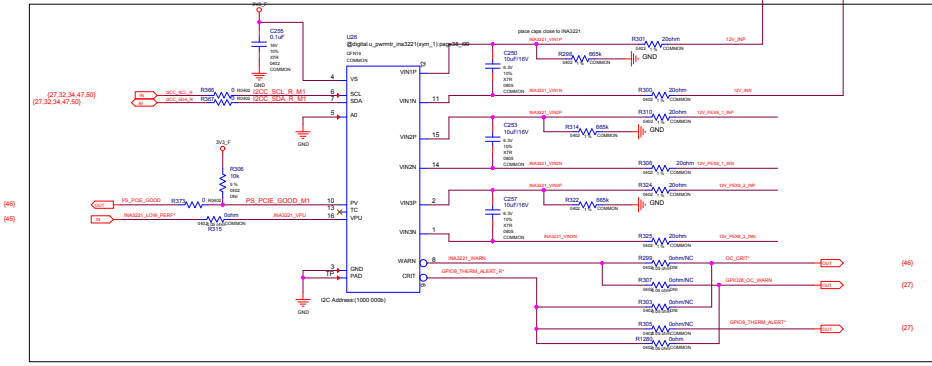
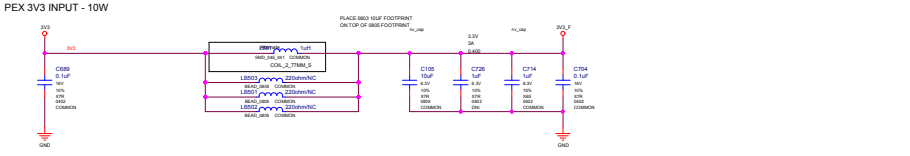
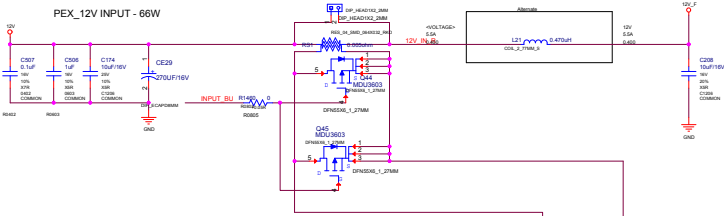
 GALAXY		Galaxy Microsystems (HK) Ltd.	
Page Name: PS: Dynamic Power Balance Phases			
Size: Custom	Project Name: P252	Design By: Neston	Rev: V10
Date: Friday, March 03, 2017	Sheet: 40	of: 52	
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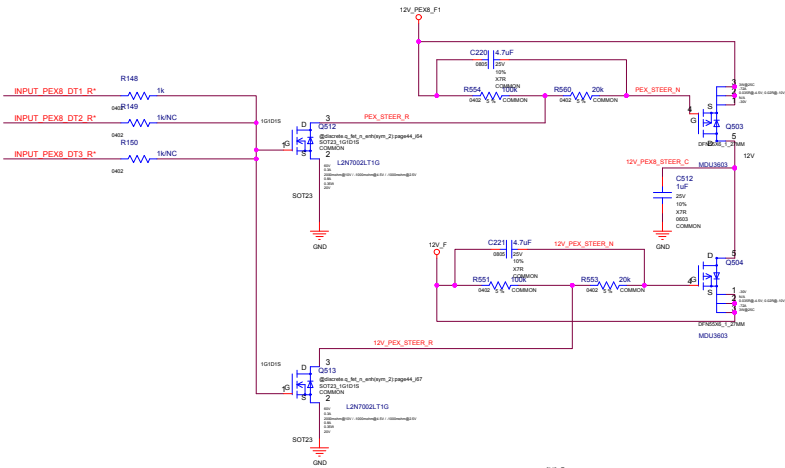


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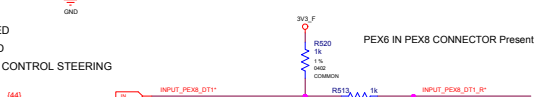
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

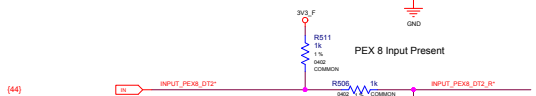
For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



PEX 6 INPUT CONNECTOR IS NOT LOADED
PEX 6 INPUT DETECT MUST BE DISABLED
PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING



NO STUFF R1
NO STUFF R2
NO STUFF C3

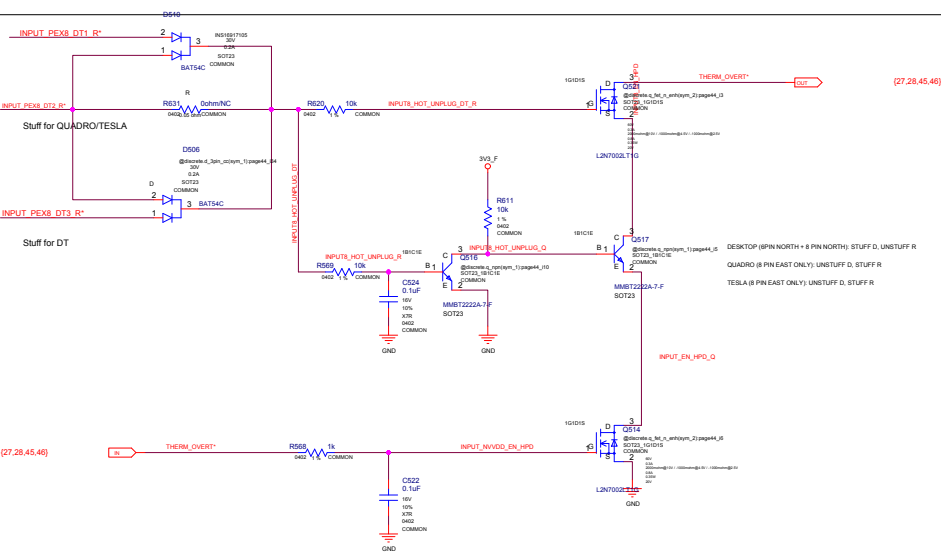


GeFORCE:

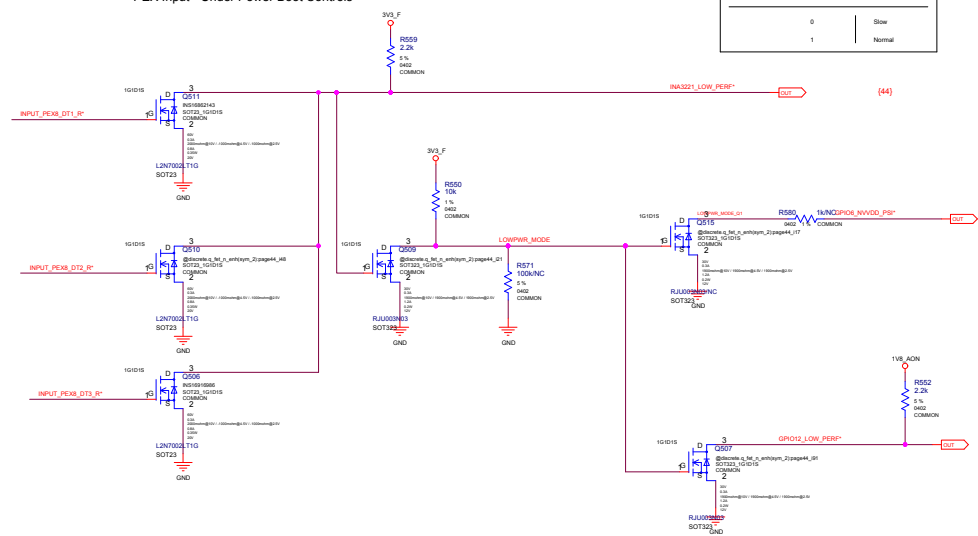
PEX 6 INPUT CONNECTOR IS LOADED
PEX 6 INPUT DETECT MUST BE USED TO ⁽⁴⁴⁾ CONTROL STEERING



STUFF R1
STUFF R2
STUFF C3



PEX Input - Under Power Boot Controls



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

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Page Name: PS: 12V Current Steering & Hot Unplug Detect

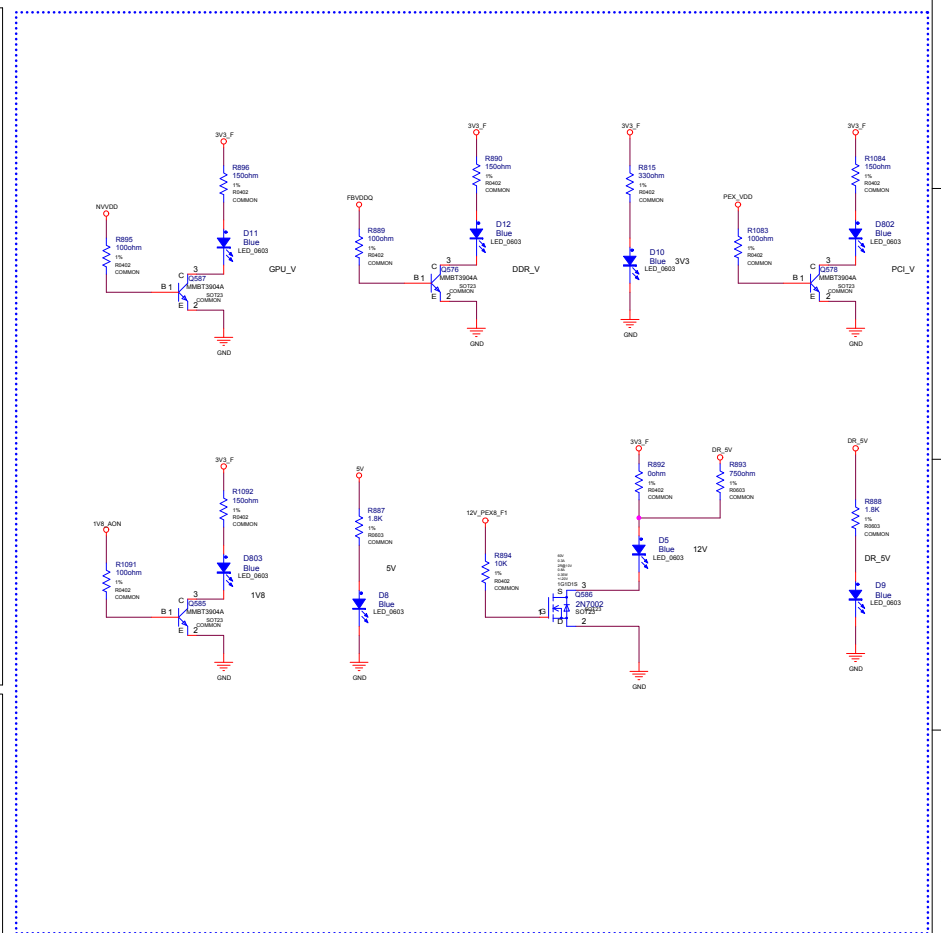
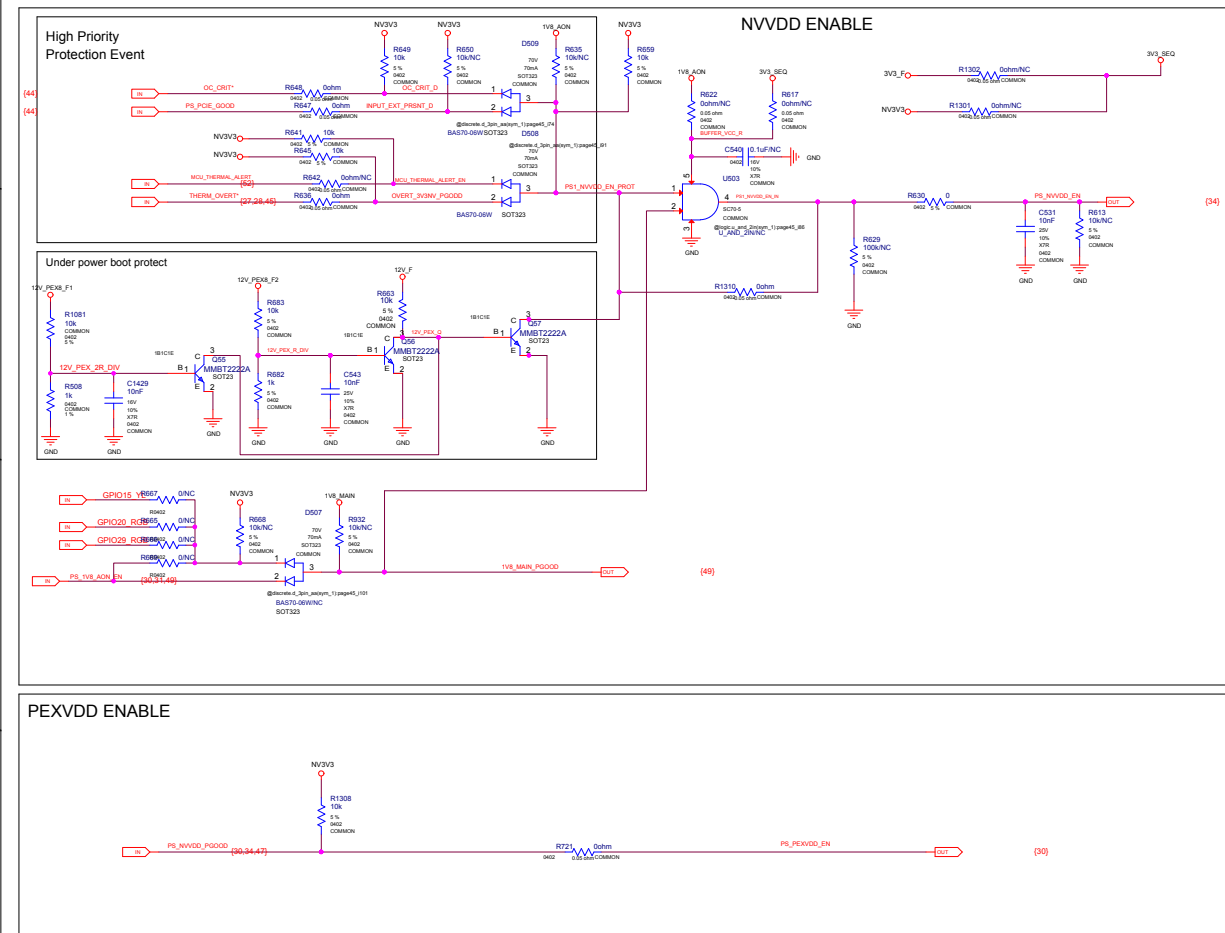
Size Custom	Project Name: P257	Design By: Neston	Rev V10
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Date:	Friday, March 03, 2017	Sheet	45	of	52
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Current Sterring. Hot Unplug



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: NVVDD ENABLE

GALAXY Galaxy Microsystems (HK) Ltd.			
Page Name: PS: NVVDD ENABLE, VOUT LED			
Size	Project Name: P25Z	Design By: Heston	Rev: V10
Customer:	Date: Friday, March 03, 2017	Sheet: 46	of 89
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[illegible]

GPU_EVENT*

The schematic diagram illustrates the FBVDD/Q ENABLE circuit. It features two input pins, [30, 34, 46] (labeled 'IN') and [30] (labeled 'IN'), which are connected to a network of resistors and capacitors. The output is a pin labeled 'PS_FBVDD_EN' (labeled 'OUT'). The circuit includes resistors R1309 (10k/1NC), R789 (10k/1NC), R774 (0ohm), and R784 (0ohm/1NC). It also includes capacitors NV2V3 and 3V3_F (5% 0402). The circuit is powered by PS_MVDD_P0200 and PEX_OVREG_P0000.

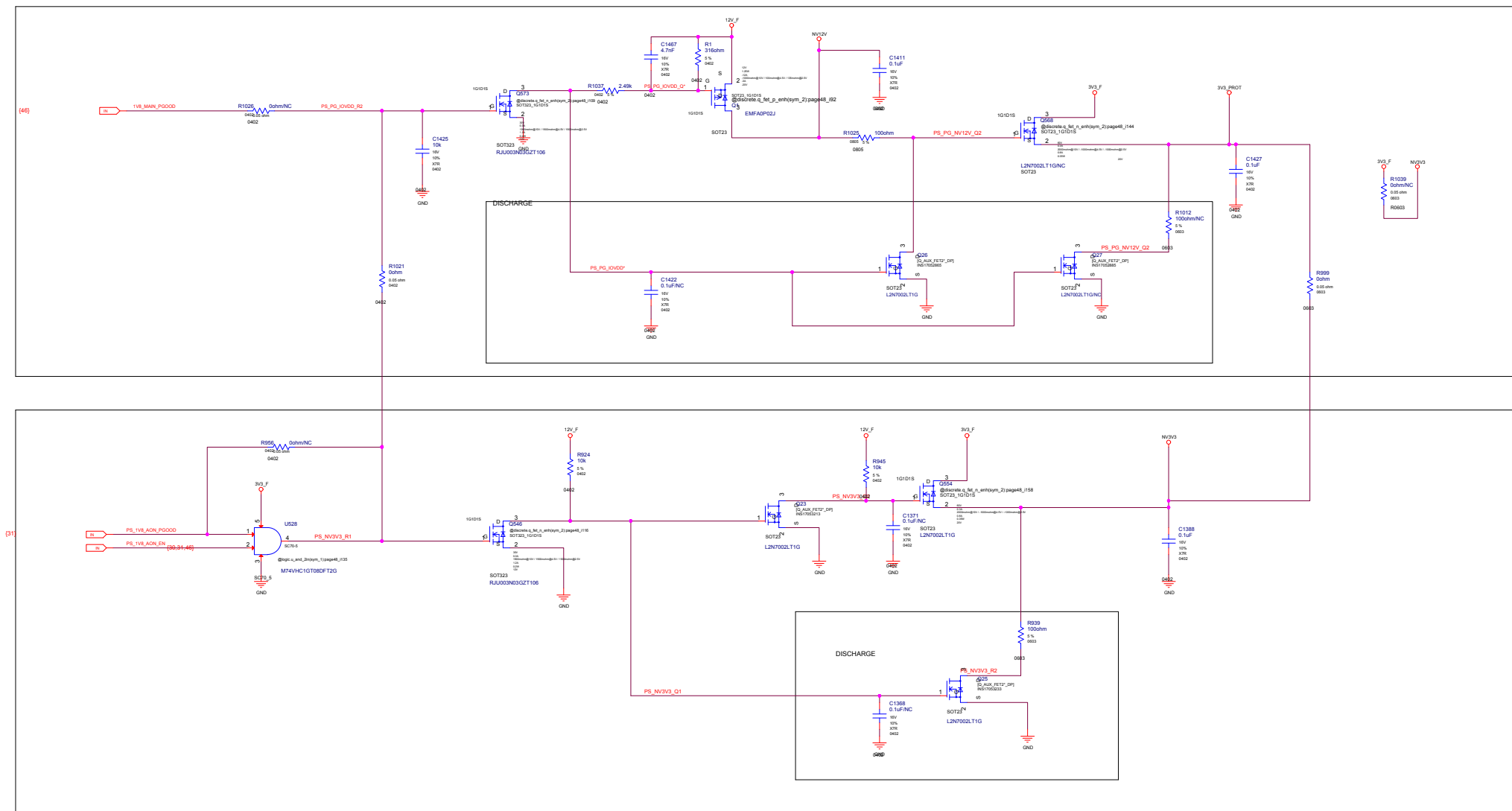
ASSEMBLY PAGE DETAIL	"ASSEMBLY DESCRIPTION" PS: G06 MISC
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The schematic diagram illustrates the LED header circuit for a GeForce GPU. The circuit is powered by a 12V source. A 10k resistor (R214) is connected to the 12V source. A 1k resistor (R233) is connected to the LED_ON pin of the AC3416L LED header. The LED header also has pins for LED_G, LED_B, and LED_R. The circuit is powered by a 12V source and grounded.

[illegible]


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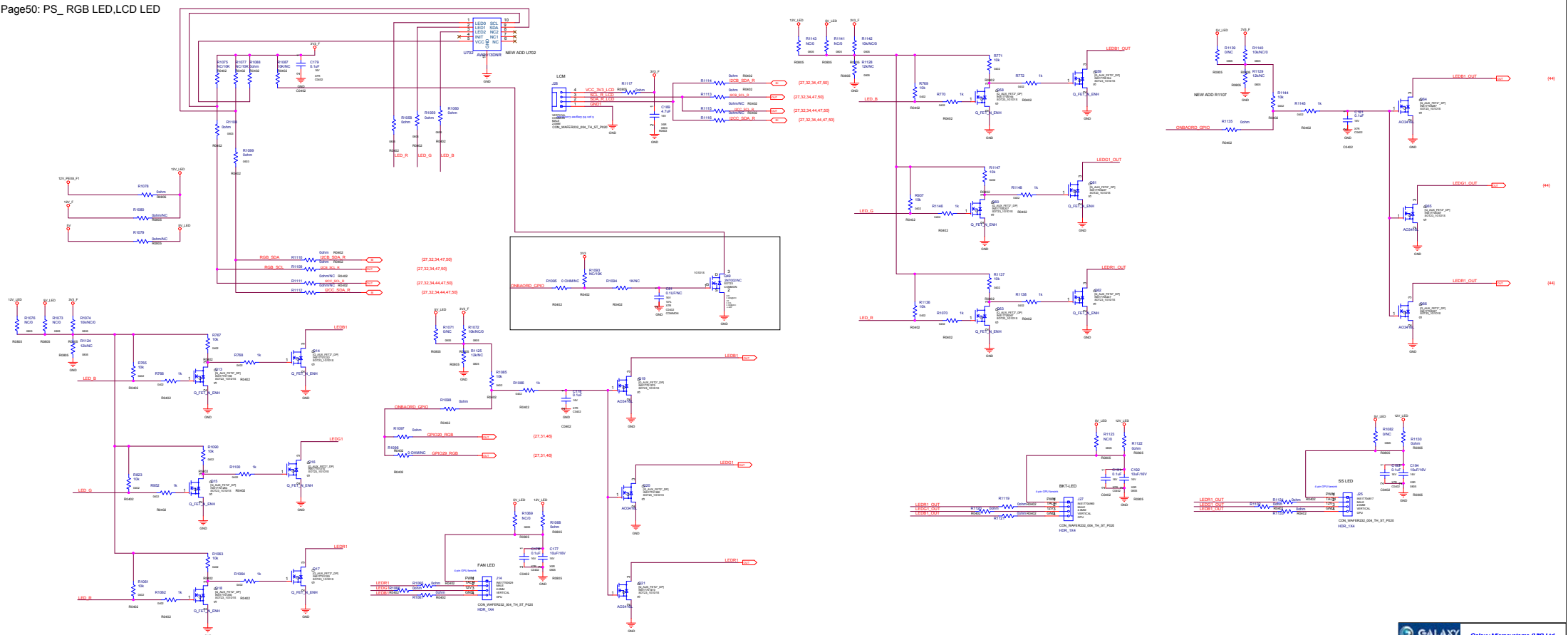
A	B	C	D	E	F	G	PROPERTY NOTE: This document contains information confidential and property to Galaxy Microsystems (HK) Ltd.
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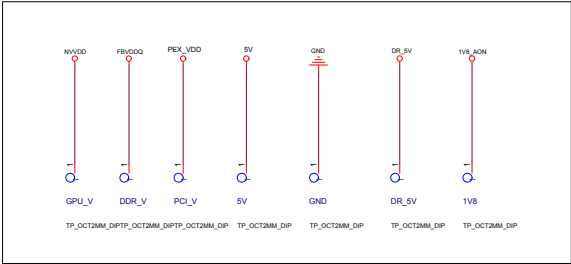
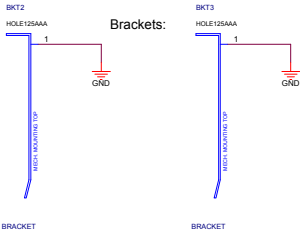


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PAGE DETAIL	PS: NV3V3, NV12V

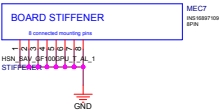
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NV3V3, NV12V			
Size Custom	Project Name: P252	Design By: Neston	Rev V10
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GPU Stiffner



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

Page Name: Mechanical: Bracket/Thermal Solution			
Size: Custom	Project Name: P25Z	Design By: Nelson	Rev: V10
Date: Friday, March 03, 2017	Sheet: 51	of: 52	
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